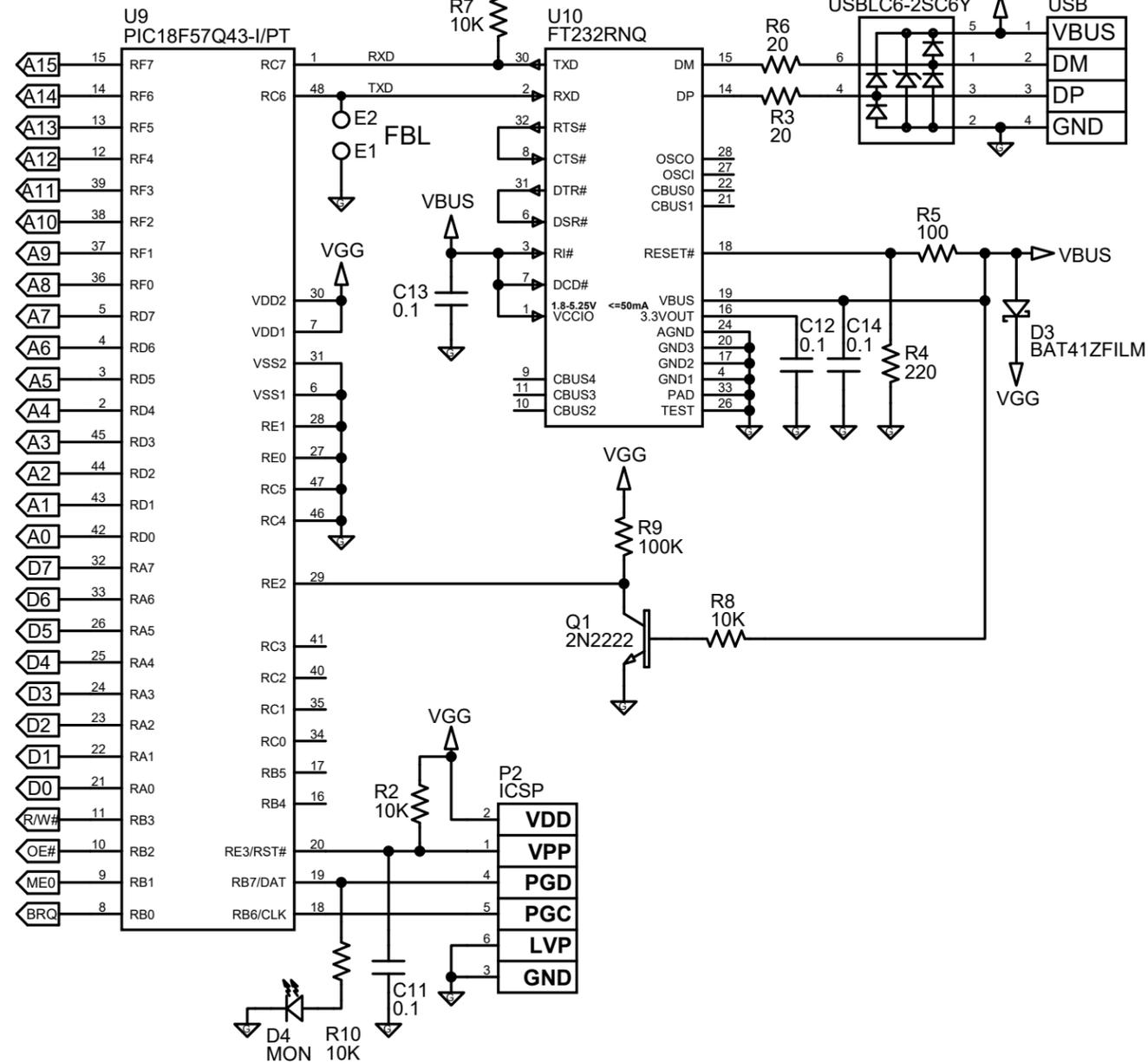
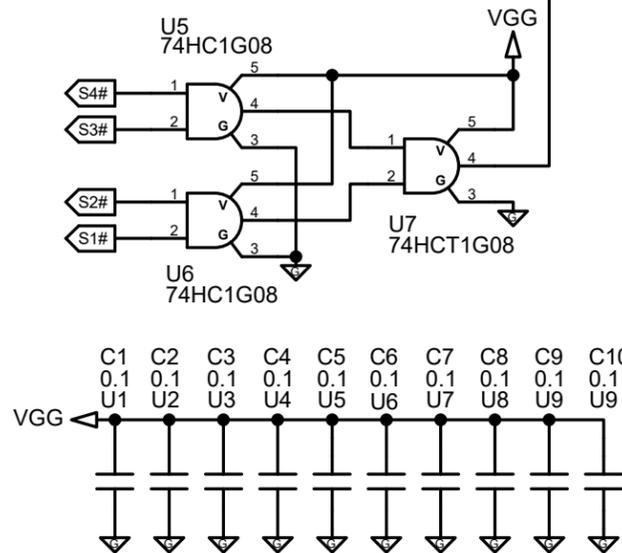
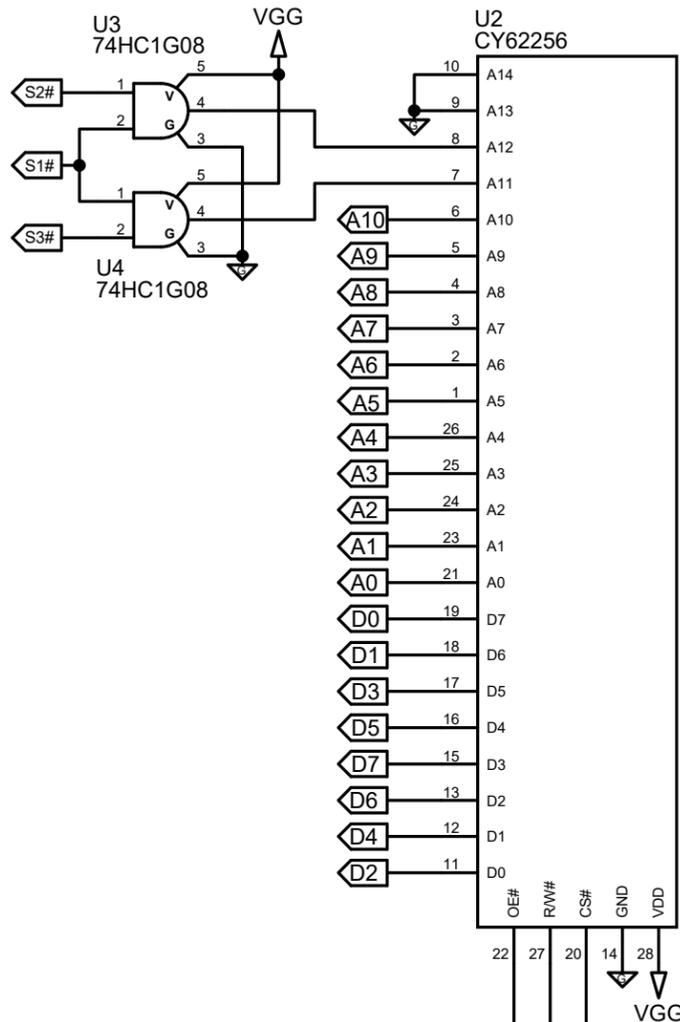
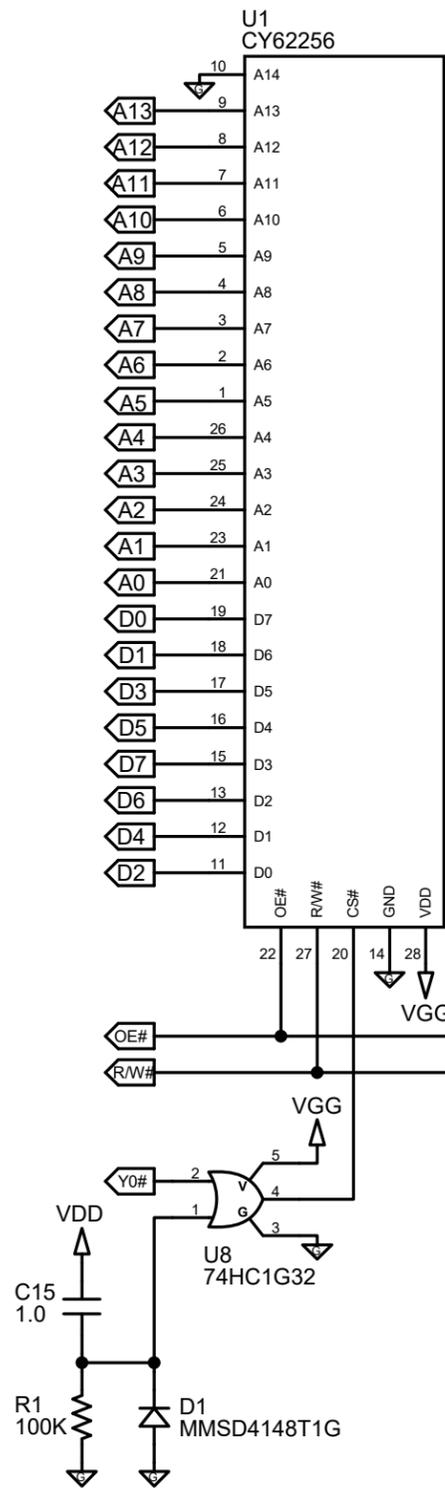
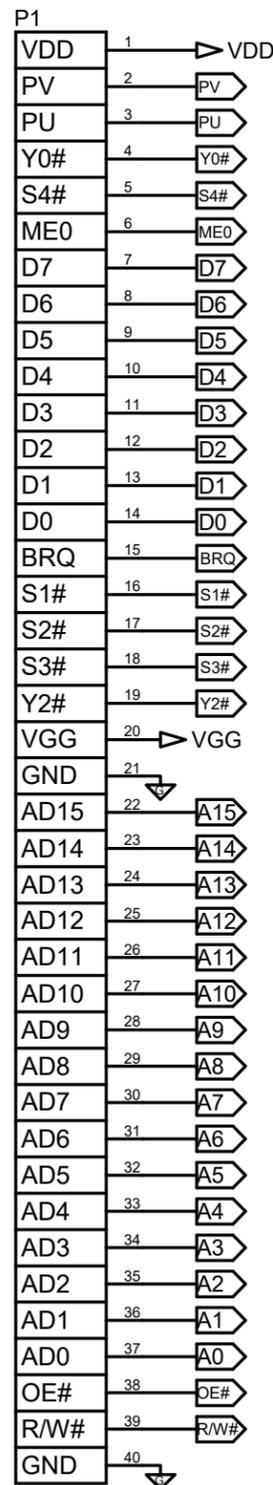
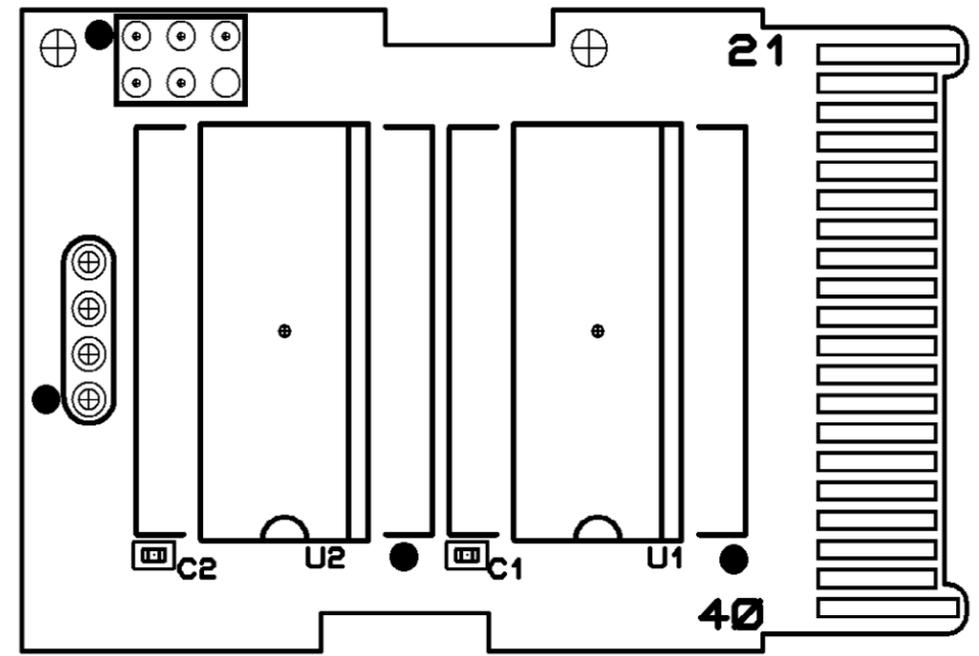
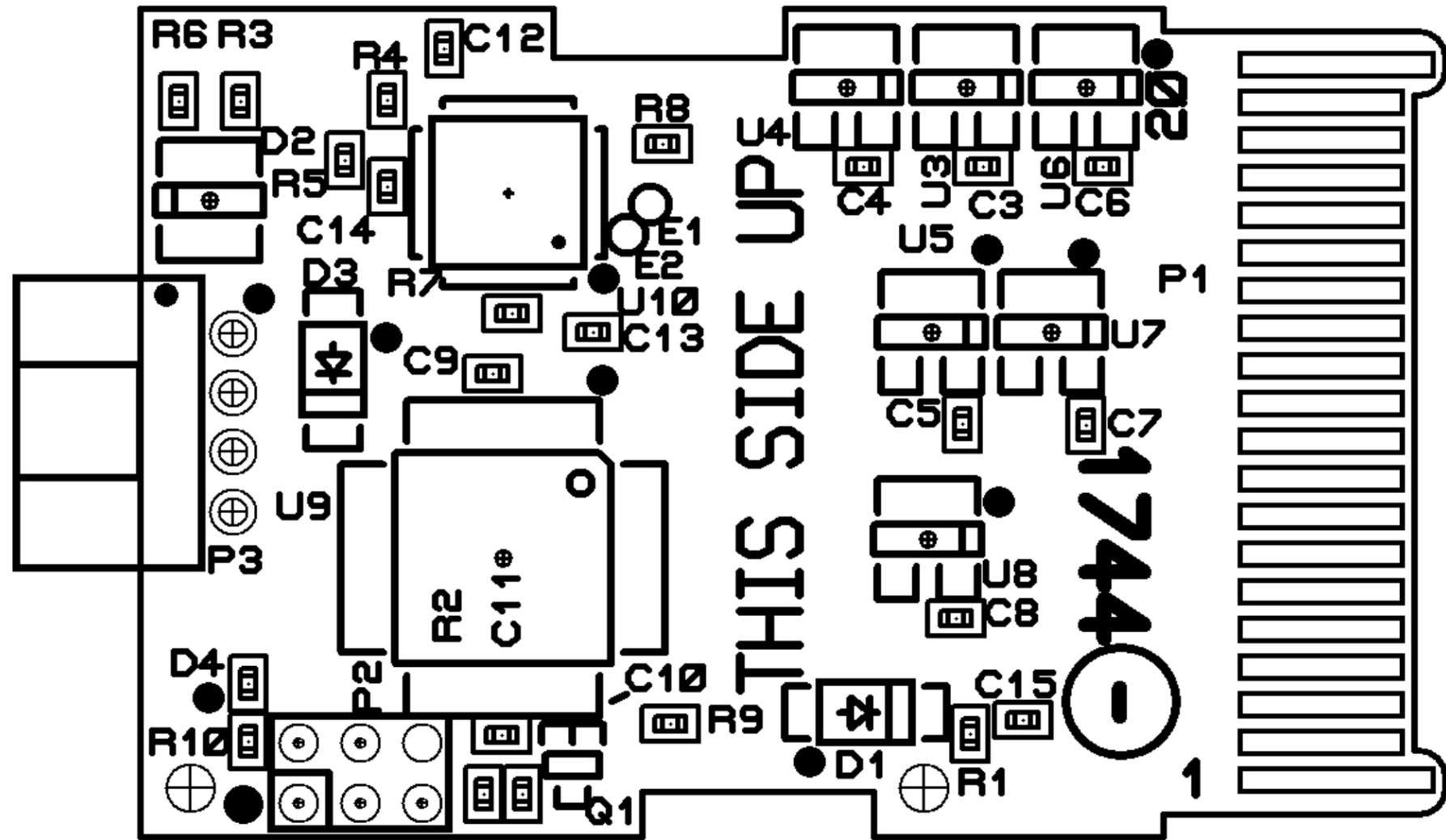


NOTES: UNLESS OTHERWISE SPECIFIED

REVISION HISTORY			
REV	DESCRIPTION	APPROVED	DATE
-	Initial release	J Taylor	2025/10/18

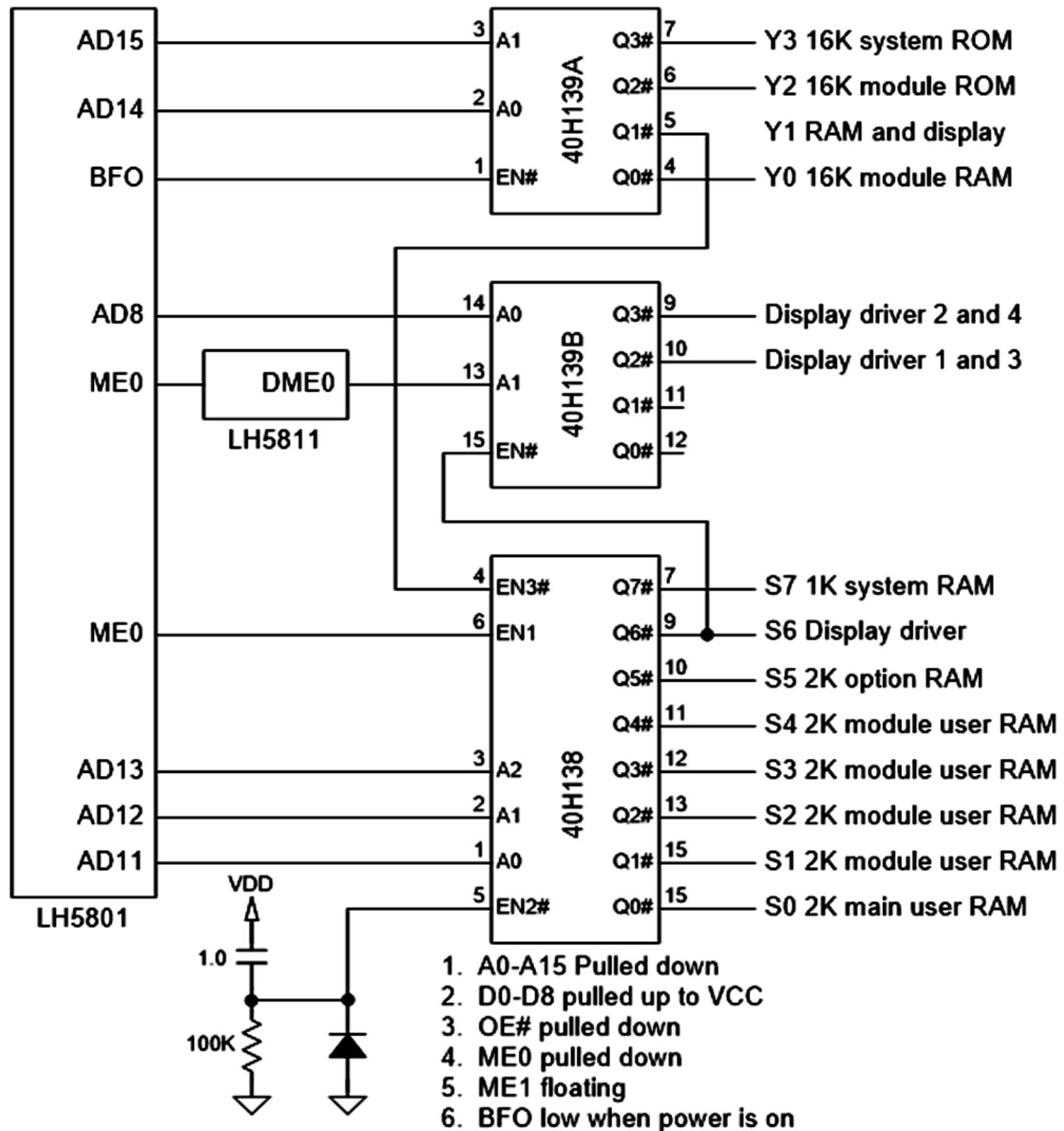


APPROVALS		DATE	TITLE
DRAWN	J TAYLOR	2025/10/18	USB loadable 24K SRAM module for TRS80 PC2
CHECKED			
ENGINEER			
PROJ ENGINEER		SIZE	FSCM NO.
APPROVED		DRAWING NO. <b>1744</b>	
GA		SCALE	NONE
		© 2025 TES	MODIFIED: 10/22/2025 11:48:19 AM
		SHEET	1 OF 4



APPROVALS		DATE	TITLE		
DRAWN	J TAYLOR	2025/10/18	Assembly		
CHECKED					
ENGINEER					
PROJ ENGINEER			SIZE	FSCM NO.	DRAWING NO.
APPROVED			B		1744
QA			SCALE	NONE	REV. -
			© 2025 TES	MODIFIED: 10/22/2025 11:48:19 AM	SHEET 2 OF 4





A15	A14	A13	A12	A0	Address Range
1	1	x	x	x	0xC000-0xFFFF
1	0	x	x	x	0x8000-0xBFFF
0	1	x	x	x	0x4000-0x7FFF
0	0	x	x	x	0x0000-0x3FFF

S6	DME0	AD8	A0	Address Range
0	1	1	1	0x7700-0x77FF
0	1	1	0	0x7600-0x76FF
0	1	1	0	0x7500-0x75FF
0	1	1	0	0x7400-0x74FF
0	1	0	1	0x7300-0x73FF
0	1	0	0	0x7200-0x72FF
0	1	0	0	0x7100-0x71FF
0	1	0	0	0x7000-0x70FF

A15	A11	A0	Address Range
0	1	1	0x7800-0x7FFF
0	1	0	0x7000-0x77FF
0	1	0	0x6800-0x6FFF
0	1	0	0x6000-0x67FF
0	1	0	0x5800-0x5FFF
0	1	0	0x5000-0x57FF
0	1	0	0x4800-0x4FFF
0	1	0	0x4000-0x47FF

APPROVALS		DATE	TITLE		
DRAWN	J TAYLOR	2025/10/18	Chip select decode on main board		
CHECKED					
ENGINEER					
PROJ ENGINEER			SIZE	FSCM NO.	DRAWING NO.
APPROVED			B		1744
QA			SCALE	NONE	REV. -
			© 2025 TES	MODIFIED: 10/22/2025 11:48:19 AM	SHEET 4 OF 4