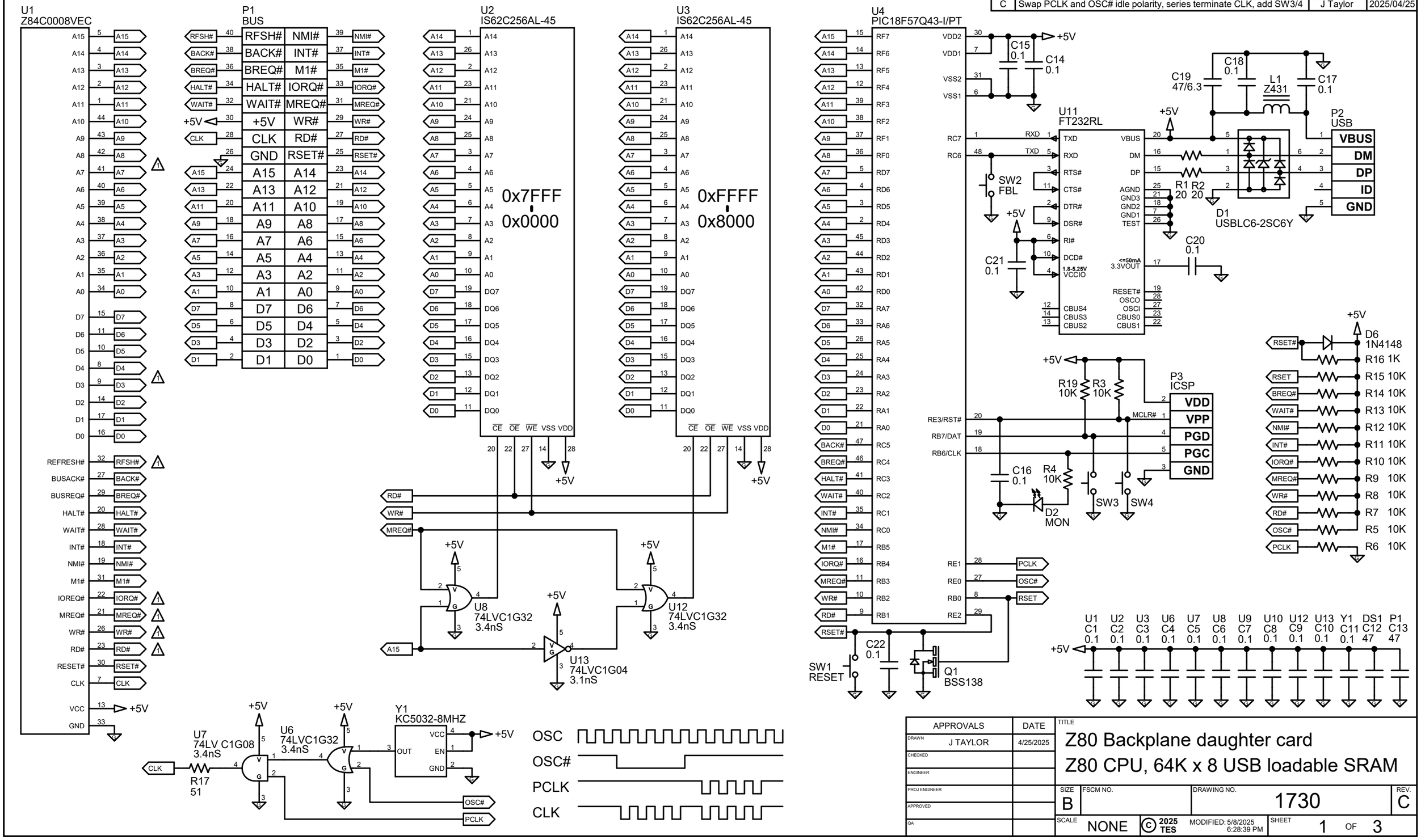
NOTES: UNLESS OTHERWISE SPECIFIED
1. These signals go Hi-Z when RESET# or BUSREQ# asserted

REVISION HISTORY			
REV	DESCRIPTION	APPROVED	DATE
-	Initial release	J Taylor	2025/03/21
A	Doubled SRAM, Added WAIT# PU, Added RSET# feedback to pic	J Taylor	2025/04/02
B	Fixed LCD decode	J Taylor	2025/04/06
C	Swap PCLK and OSC# idle polarity, series terminate CLK, add SW3/4	J Taylor	2025/04/25



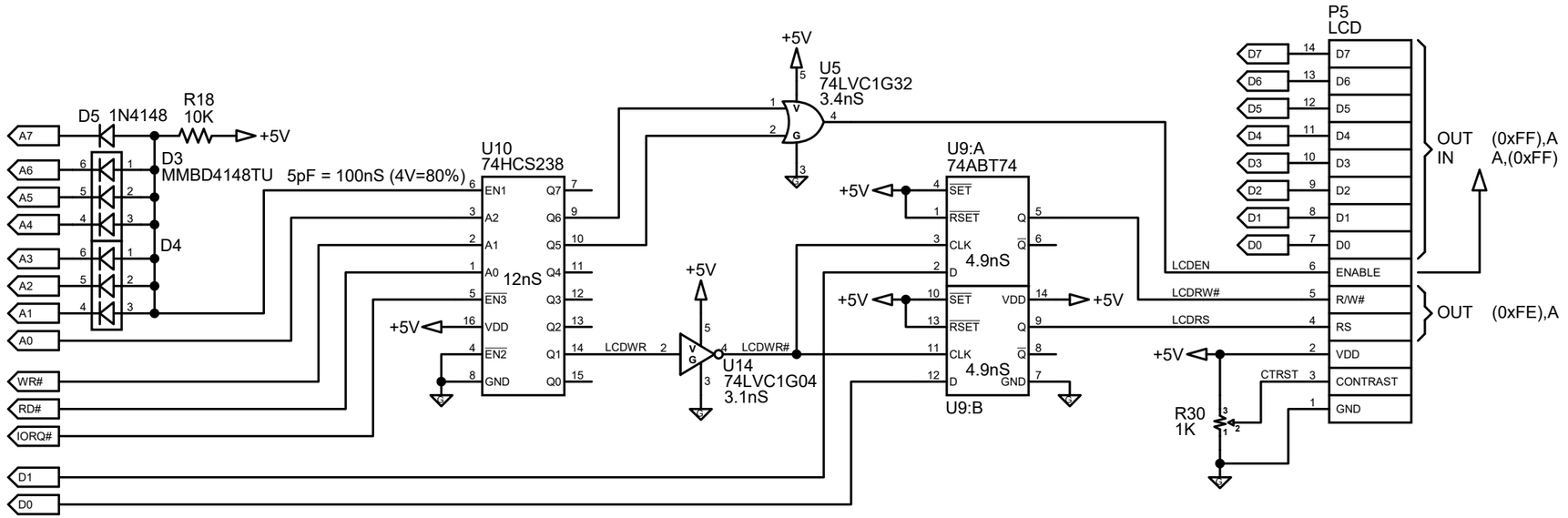
APPROVALS	DATE
DRAWN J TAYLOR	4/25/2025
CHECKED	
ENGINEER	
PROJ ENGINEER	
APPROVED	
QA	

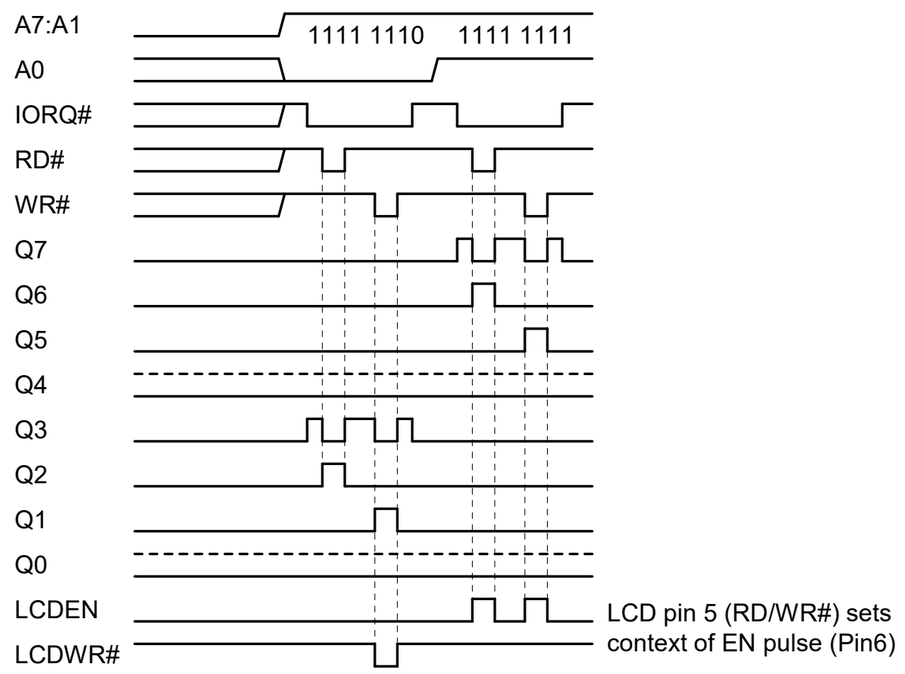
TITLE
Z80 Backplane daughter card
Z80 CPU, 64K x 8 USB loadable SRAM

SIZE	FSCM NO.	DRAWING NO.	REV.
B		1730	C

SCALE NONE | © 2025 TES | MODIFIED: 5/8/2025 6:28:39 PM | SHEET 1 OF 3

NOTES: UNLESS OTHERWISE SPECIFIED



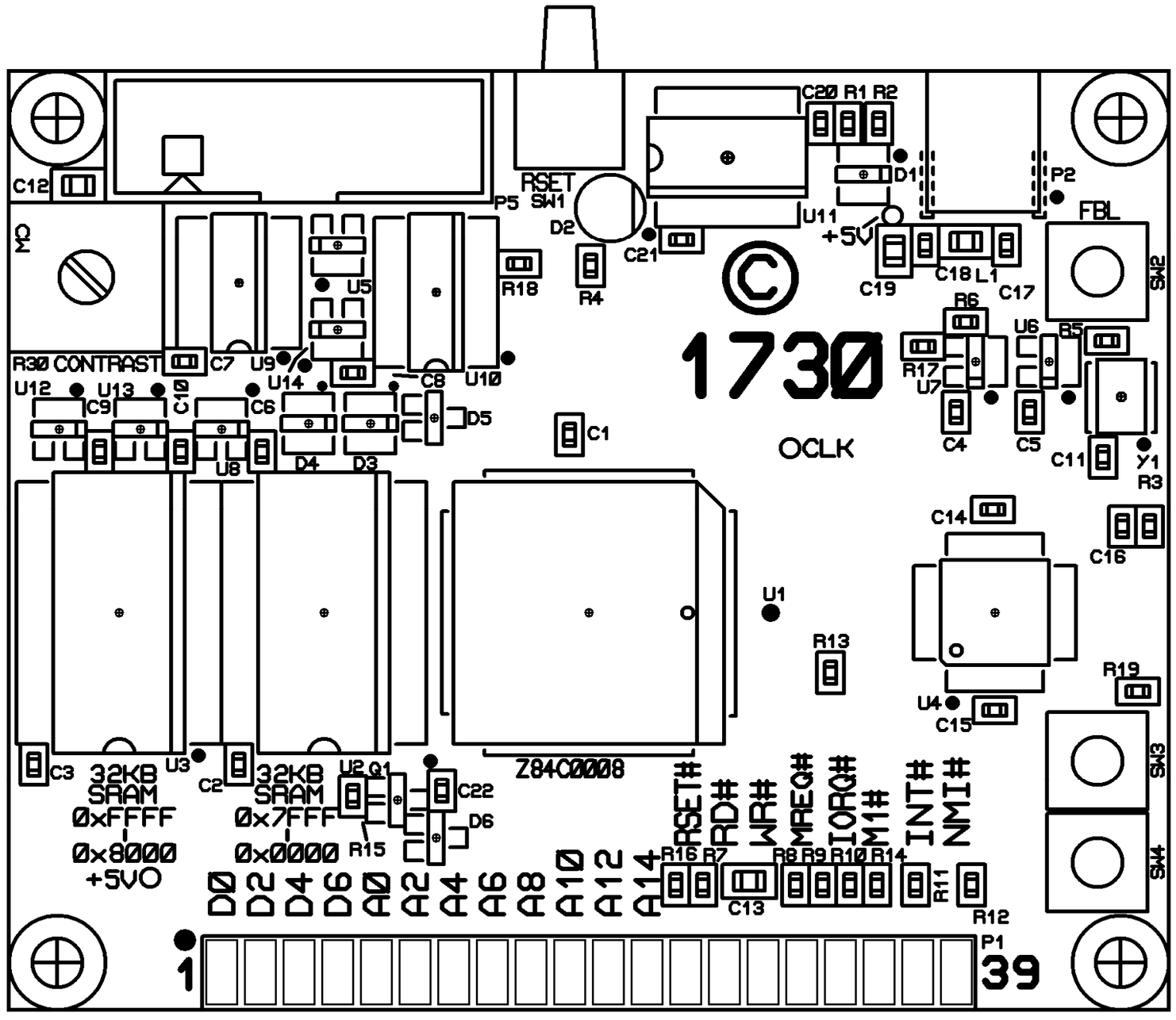


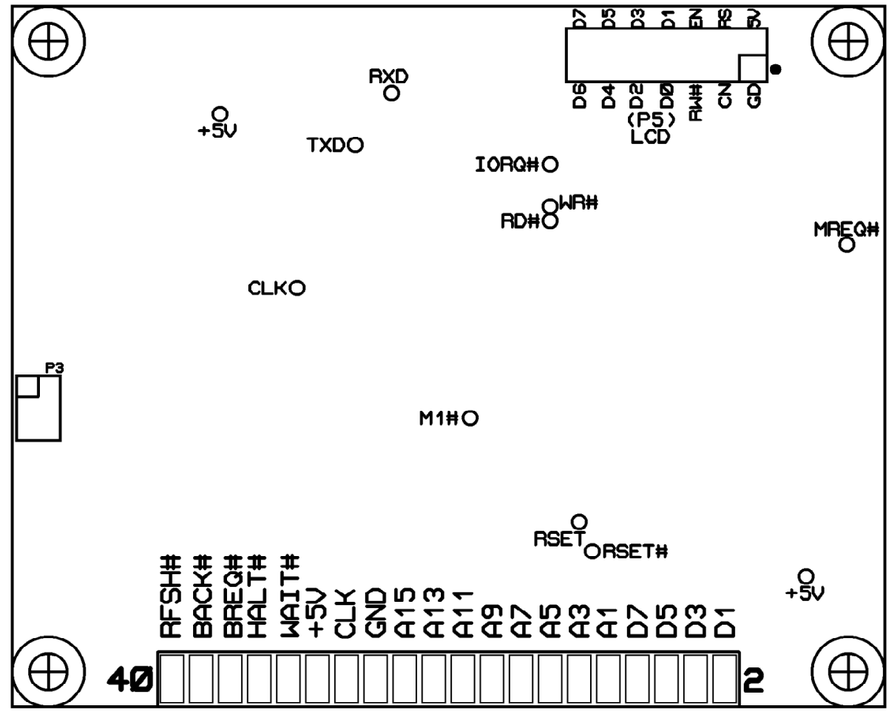
APPROVALS	DATE	TITLE
DRAWN J TAYLOR	4/25/2025	LCD Interface
CHECKED		
ENGINEER		
PROJ ENGINEER		
APPROVED		
QA		

SIZE	FSCM NO.	DRAWING NO.	REV.
B		1730	C

SCALE		MODIFIED:	SHEET
NONE	© 2025 TES	5/8/2025 6:28:39 PM	2 OF 3

NOTES: UNLESS OTHERWISE SPECIFIED





APPROVALS	DATE	TITLE
DRAWN J TAYLOR	4/25/2025	Assembly Drawing
CHECKED		
ENGINEER		
PROJ ENGINEER		
APPROVED		
QA		

SIZE	FSCM NO.	DRAWING NO.	REV.
B		1730	C

SCALE		MODIFIED:	SHEET
NONE	© 2025 TES	5/8/2025 6:28:39 PM	3 OF 3