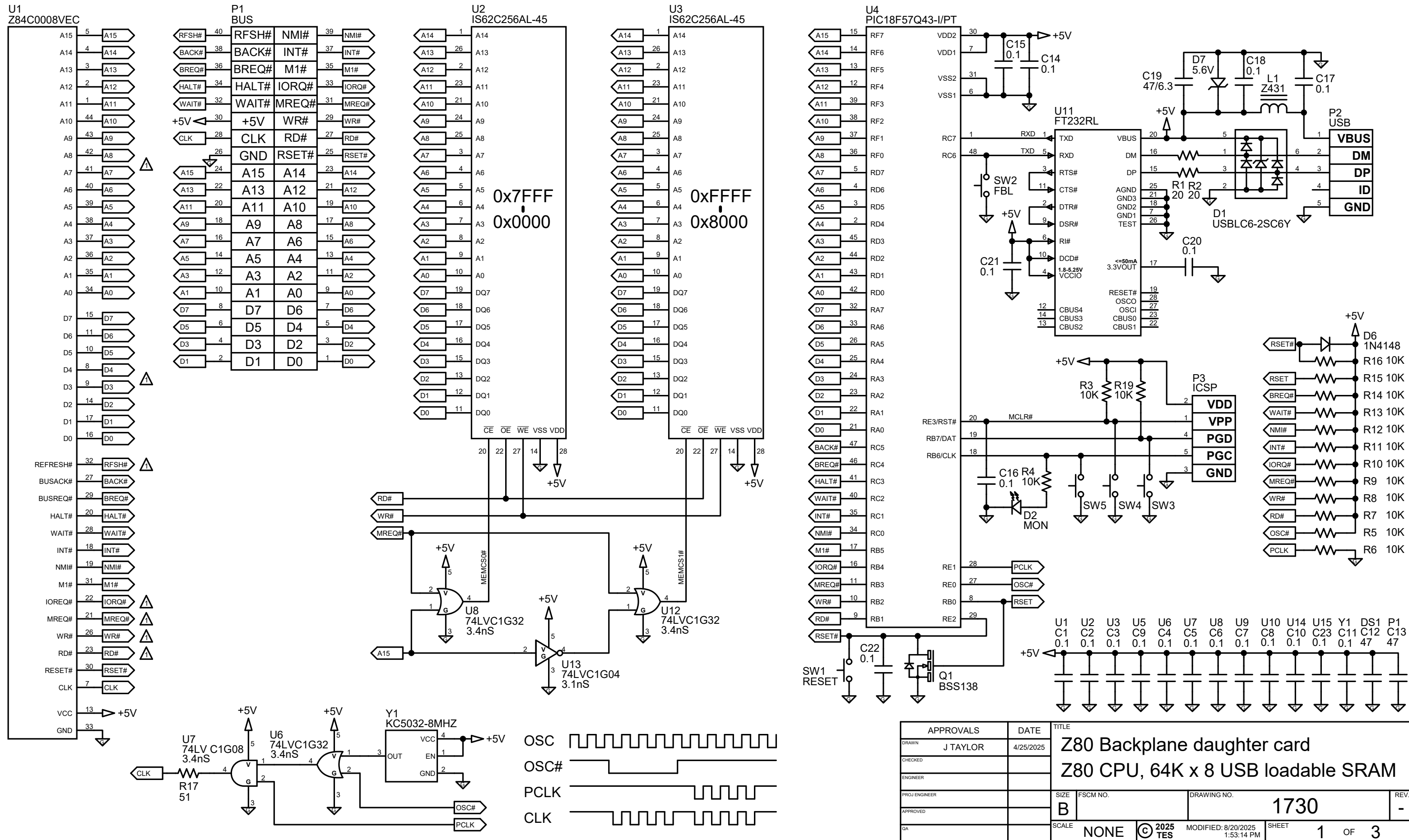
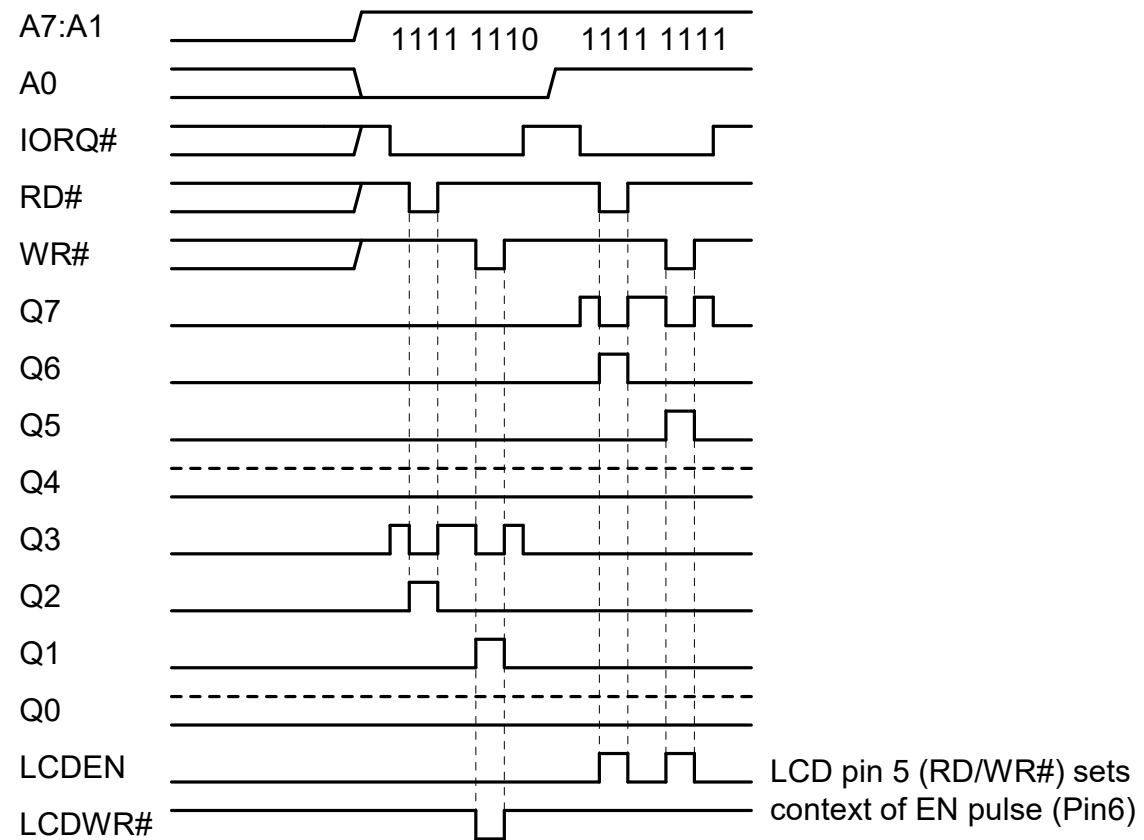
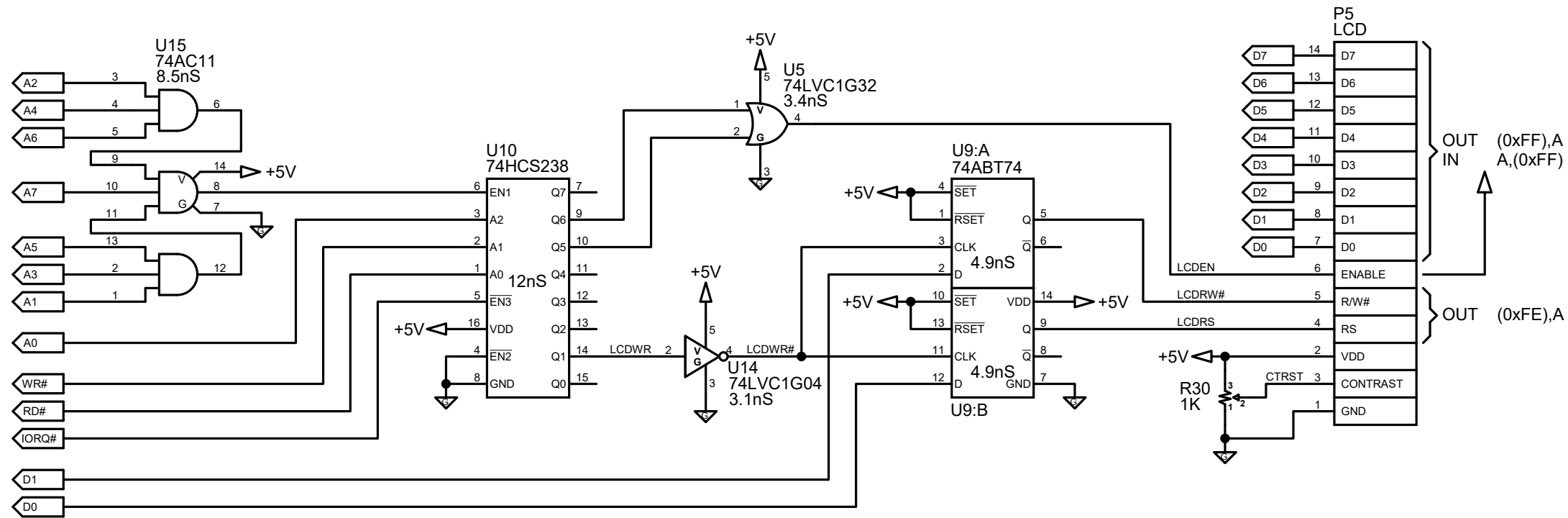


NOTES: UNLESS OTHERWISE SPECIFIED
 1. These signals go Hi-Z when RESET# or BUSREQ# asserted

REVISION HISTORY			
REV	DESCRIPTION	APPROVED	DATE
-	Initial release	J Taylor	2025/08/06



APPROVALS		DATE	TITLE
DRAWN	J TAYLOR	4/25/2025	Z80 Backplane daughter card
CHECKED			Z80 CPU, 64K x 8 USB loadable SRAM
ENGINEER			
PROJ ENGINEER			SIZE FSCM NO. DRAWING NO.
APPROVED			B 1730
GA			SCALE NONE © 2025 TES MODIFIED: 8/20/2025 1:53:14 PM SHEET 1 OF 3



APPROVALS		DATE	TITLE		
DRAWN	J TAYLOR	4/25/2025	LCD Interface		
CHECKED					
ENGINEER					
PROJ ENGINEER			SIZE	FSCM NO.	DRAWING NO.
APPROVED			B		1730
QA			SCALE	NONE	REV. -
			© 2025 TES	MODIFIED: 8/20/2025 1:53:14 PM	SHEET 2 OF 3

