PIC18F66K80 Family Silicon Errata and Data Sheet Clarifications

PIC18F66K80 Family

Product Page Links

Introduction

The PIC18F66K80 devices that you have received conform functionally to the current device data sheet (DS30009977**G**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F66K80 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID				
		A2	A3	A4	A6	A7
PIC18F66K80	0x60E0	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18F65K80	0x6140	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18F46K80	0x6100	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18F45K80	0x6160	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18F26K80	0x6120	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18F25K80	0x6180	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18LF66K80	0x61C0	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18LF65K80	0x6220	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18LF46K80	0x61E0	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18LF45K80	0x6240	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18LF26K80	0x6200	0x0002	0x0003	0x0004	0x0006	0x0007
PIC18LF25K80	0x6260	0x0002	0x0003	0x0004	0x0006	0x0007

Important: Refer to the **Device/Revision ID** section in the device data sheet for more detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions				
				A2	A3	A4	A6	A7
Analog-to-Digital Converter (ADC)	ADC Performance	1.1.1	The 12-Bit ADC Performance is Outside the Data Sheet's Specifications	X	X	X	X	X
Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)	Synchronous Transmit	1.2.1	Transmitted Data May Become Corrupted in Synchronous Transmit Mode	X				
	Receive Interrupt	1.2.2	Unintended Double Execution of the CALL Instruction	X	X	X	X	X
Enhanced Capture Compare PWM (ECCP)	Auto-Shutdown	1.3.1	The PWM's Tri-State Setting of the Auto-Shutdown Feature Will Not Drive the Pin to Tri-State	X	X	X	X	X
Enhanced Controller Area Network (ECAN)	CAN Clock Source Selection	1.4.1	The CLKSEL Bit in the CIOCON Register is Modifiable While the ECAN Module is Active	X				
	Enhanced Window Address (EWIN)	1.4.2	The EWIN Feature Will Not Move the BnCON[0...5] Registers Into the Access Window of RAM	X				
	Disable/Sleep Mode	1.4.3	Disable/Sleep Mode Reverts CANTX Control to TRISx/LATx Instead of Going to Recessive State	X	X	X	X	X
	CLKSEL Bit	1.4.4	Setting the CLKSEL Bit of CIOCON Can Occasionally Lead to Missed Incoming CAN Messages	X	X	X	X	X
Ultra Low-Power Sleep	Sleep Entry	1.5.1	Entering Ultra Low-Power Sleep Mode By Setting $\overline{\text{RETEN}}$ = 0 and $\overline{\text{SRETEN}}$ = 1Will Cause the Device to Become Unprogrammable Through ICSP™	X				
Electrical Specifications	I_{PD}/I_{DD} Maximum Limits	1.6.1	Maximum Current Limits May Be Higher Than Specified In the Data Sheet	X				
Resets	BOR Enable/ Disable	1.7.1	An Unexpected Reset May Occur if the BOR Module is Disabled and Then Re-Enabled When the HLVD Module is Not Enabled	X	X	X	X	X
	Master Clear Enable	1.7.2	The $\overline{\text{MCLR}}$ Pin Will Not Be Readable When MCLRE = 0 for All 28-Pin Variants	X	X	X	X	X
Timer1/3	Gated Enable	1.8.1	Timer1/3 Gate Control Will Not Function Up to the Speed of F_{OSC} When TxCON is Set to the System Clock	X	X			
	Interrupt	1.8.2	Unexpected Interrupt Flag Generation May Occur in Asynchronous External Input Mode	X	X	X	X	X
Primary Oscillator	XT Mode	1.9.1	XT Primary Oscillator Mode Does Not Reliably Function When the Driving Crystals are Above 3 MHz	X	X	X		
Instruction Set	PUSHL Instruction	1.10.1	The PUSHL instruction incorrectly executes	X	X	X	X	X

Table 2. Silicon Issue Summary (continued)

Module	Feature	Item No.	Issue Summary	Affected Revisions				
				A2	A3	A4	A6	A7

Note: Only those issues indicated in the last column apply to the current silicon revision.

1. Silicon Errata Issues

NOTICE This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1. Module: Analog-to-Digital Converter (ADC)

1.1.1. The 12-Bit ADC Performance is Outside the Data Sheet's Specifications

The 12-bit ADC performance is outside the data sheet's ADC specifications. When used as a 12-bit ADC, the possible issues are:

- High offset error:
  - up to a maximum of ±25 LSb at 25°C
  - up to a maximum of ±30 LSb at -40°C, 85°C, and 125°C
- High DNL error:
  - up to a maximum of +6.0/-4.0 LSb
- Multiple missing codes:
  - up to a maximum of 20 missing codes

Users should evaluate the 12-bit ADC performance in their application using the suggested work around. See table below for guidance specifications.

Reduced bit resolution specifications can be derived by dividing, as appropriate. For instance, 10-bit guidance is obtained by dividing the parameters in the table below by four.

Table 1-1. ADC Characteristics

Standard Operating Conditions (unless otherwise stated)							
Param No.	Sym.	Characteristics	Min.	Typ†	Max.	Units	Conditions
A01	N_R	Resolution	—	—	12	bit	$\Delta V_{REF} \geq 5.0V$
A02	E_{IL}	Integral Linearity Error	—	—	±10	LSb	$\Delta V_{REF} \geq 5.0V$
A04	E_{DL}	Differential Linearity Error	—	—	+6.0/-4.0	LSb	$\Delta V_{REF} \geq 5.0V$
A06	E_{OFF}	Offset Error	—	—	±25	LSb	$\Delta V_{REF} \geq 5.0V$, 25°C
			—	—	±30	LSb	$\Delta V_{REF} \geq 5.0V$, -40°C, 85°C, 125°C
A07	E_{GN}	Gain Error	—	—	±15	LSb	$\Delta V_{REF} \geq 5.0V$
A10	—	Monotonicity(1)	—	—	—	—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	ΔV_{REF}	Reference Voltage Range (V_{REFH} - V_{REFL})	3	—	AV_{DD} - AV_{SS}	V	
A21	V_{REFH}	Reference Voltage High	AV_{SS} + 3.0V	—	AV_{DD} + 0.3V	V	
A22	V_{REFL}	Reference Voltage Low	AV_{SS} - 0.3V	—	AV_{DD} - 3.0V	V	
A25	V_{AIN}	Analog Input Voltage	V_{REFL}	—	V_{REFH}	V	

Note:
1. The ADC conversion result never decreases with an increase in the input voltage.

Work around

Calibrate for offset in Single-Ended mode by connecting a positive ADC input to ground and taking the reading. This will be the offset of the device and can be used to compensate for the subsequent readings on the actual inputs.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.2. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

1.2.1. Transmitted Data May Become Corrupted in Synchronous Transmit Mode

In Synchronous Transmit mode, data may be corrupted if using the TXxIF bit to determine when to load the TXREGx register. One or more of the intended transmit messages may be incorrect.

Work around

A fixed delay added before loading TXREGx may not be a reliable work around. When loading TXREGx, check that the TRMT bit in the TXSTAx register is set instead of checking the TXxIF bit. The following code can be used:

```
while(!TXSTAxbits.TRMT);
// wait to load TXREGx until TRMT is set
```

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X							

1.2.2. Unintended Double Execution of the `CALL` Instruction

The `CALL` function will be executed twice if the following conditions are met:

- EUSART Receive Interrupt is enabled (RCIE = `1`)
- EUSART is disabled (SPEN = `0`) as the Receive Interrupt (RCIF) is set within the same clock cycle
- The next instruction is a function call (`CALL` function)

Work around

Disable the Receive Interrupt (RCIE = `0`) prior to turning off the EUSART module.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.3. Module: Enhanced Capture Compare PWM (ECCP)

1.3.1. The PWM's Tri-State Setting of the Auto-Shutdown Feature Will Not Drive the Pin to Tri-State

The tri-state setting of the auto-shutdown feature in the enhanced PWM will not successfully drive the pin to tri-state. The pin will remain an output and should not be driven externally. All tri-state settings will be affected.

Work around

Use one of the other two auto-shutdown states available as outlined in the data sheet.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.4. Module: Enhanced Controller Area Network (ECAN)

1.4.1. The CLKSEL Bit in the CIOCON Register is Modifiable While the ECAN Module is Active

The CLKSEL bit in the CIOCON register remains modifiable while the ECAN module is not in Configuration mode. Accidental state changes of this bit will result in immediate bit clock changes that will affect all nodes on the bus.

Work around

While the ECAN module is in Run mode, do not modify the state of the CLKSEL bit unless the ECAN module is first changed into Configuration mode.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X							

1.4.2. The EWIN Feature Will Not Move the BnCON[0...5] Registers Into the Access Window of RAM

The Enhanced Window Address (EWIN) feature will not move the BnCON[0...5] registers into the access window of RAM. The rest of the registers in B0 through B5 will be transferred into the access bank successfully. This feature is only available in Mode 1 and Mode 2; Mode 0 applications will not be affected.

Work around

1. Set the ECANCON register's EWIN bits to the desired buffer:

```
ECANCONbits.EWIN = Buffer_Selection;
```

2. Decode the desired buffer to each individual Buffer Control register, BnCON[0...5]:

```
switch(Buffer_Selection)
{
    case 18:        // EWIN code for Buffer B0
            break;
    case 23:        // EWIN code for Buffer B5
            break;
    default:
            break;
}
```

3. Process information in the selected buffer control register. Note that the BnCON[0...5] Control registers can be set up for either transmit or receive operations:

```
case 18:      // Save B0CON and clear flags being processed
temp = B0CON;   // Clear any flags
break;
```

4. Continue processing the rest of the buffer in the windowed location.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X							

1.4.3. Disable/Sleep Mode Reverts CANTX Control to TRISx/LATx Instead of Going to Recessive State

When the ECAN module is placed into Disable/Sleep mode, the CANTX pin will revert to being controlled by the PORTx/TRISx/LATx registers instead of remaining in the Recessive state as intended.

Work around

If Disable/Sleep mode of the ECAN is to be used, set the TRIS bit associated with the TX pin (either TRSIB2 if the CANMX Configuration bit is set, TRISC6 if the CANMX bit is cleared on the 28-pin and 40/44-pin packages, or TRISE4 if the CANMX Configuration bit is cleared on 64-pin packages) and ensure that the CANTX line has a proper pull-up to V_{DD}. This will ensure that, when the pin is controlled by TRIS/LAT settings, it will be pulled to the CAN Recessive state and not cause issues on the CAN bus.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.4.4. Setting the CLKSEL Bit of CIOCON Can Occasionally Lead to Missed Incoming CAN Messages

A very small number of CAN applications are experiencing a low failure rate when the microcontroller core is clocked by an oscillator through a PLL (either the PLLCFG bit is cleared or PLLEN bit of OSCTUNE is set) and the ECAN module is clocked by the same source without a PLL (the CLKSEL bit of CIOCON is set). This failure mechanism is characterized by incoming CAN messages rarely being missed, with the ECAN module acknowledging the incoming message on the bus but not triggering interrupts or transferring the incoming data into the receive buffers.

Work around

If it is essential that the application never misses a message, it is recommended that both the ECAN module and the microcontroller be clocked either through the PLL or without a PLL. This can be achieved by ensuring that the CLKSEL bit of CIOCON remains cleared.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.5. Module: Ultra Low-Power Sleep

1.5.1. Entering Ultra Low-Power Sleep Mode By Setting $\overline{\text{RETEN}}$ = 0 and $\overline{\text{SRETEN}}$ = 1Will Cause the Device to Become Unprogrammable Through ICSP™

Entering Ultra Low-Power Sleep mode by setting $\overline{\text{RETEN}}$ = `0` and $\overline{\text{SRETEN}}$ = `1` will cause the device to not be programmable through ICSP™. This issue occurs when the $\overline{\text{RETEN}}$ bit in CONFIG1L is cleared to `'0'`, the $\overline{\text{SRETEN}}$ bit in the WDTCON register is set to `'1'` and a `SLEEP` instruction is executed within the first 350 µs of code execution. This happens after a Reset event, causing the device to enter Ultra Low-Power Sleep mode.

Work around

Use Normal Sleep and Low-Power Sleep modes only, or on any Reset, ensure that at least 350 µs pass before executing the `SLEEP` instruction when ULP is enabled. To ensure the Ultra Low-Power Sleep mode is not enabled, the $\overline{\text{RETEN}}$ bit in CONFIG1L should be set to a `'1'` and the $\overline{\text{SRETEN}}$ bit in the WDTCON register should be cleared to a `'0'`. The following code can be used:

```
// This will ensure the RETEN bit is set to '1'
#pragma config RETEN = OFF
// This will ensure that the SRETEN bit is '0'
WDTCONbits.SRETEN = 0;
```

If the Ultra Low-Power Sleep mode is needed, the user must ensure that the minimum time, before the first `SLEEP` instruction is executed, is greater than 350 µs.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			

X							

1.6. Module: Electrical Specifications

1.6.1. Maximum Current Limits May Be Higher Than Specified In the Data Sheet

The I_{DD} and I_{PD} limits do not match the data sheet.

All I_{DD} maximum limits will equal 2.8 times the values listed in the data sheet.

The I_{PD} values, shown in **bold** in the table below, reflect the updated silicon maximum limits.

Table 1-2. 31.2 DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended)

PIC18F66K80 (Industrial/ Extended)		Standard Operating Conditions (unless otherwise stated)				
Param No.	**Device**	**Typ.**	**Max.**	**Units**	**Conditions**	
	Power-Down Current (I_{PD})(1)					
	PIC18LFXXK80	0.008	**7**	µA	-40°C	V_{DD} = 1.8V(4) (Sleep mode) Regulator Disabled
		0.013	**7**	µA	+25°C	
		0.035	**9**	µA	+60°C	
		0.218	**10**	µA	+85°C	
		3	**12**	µA	+125°C	
	PIC18LFXXK80	0.014	**8**	µA	-40°C	V_{DD} = 3.3V(4) (Sleep mode) Regulator Disabled
		0.034	**8**	µA	+25°C	
		0.092	**9**	µA	+60°C	
		0.312	**10**	µA	+85°C	
		4	**16**	µA	+125°C	
	PIC18FXXK80	0.2	**9**	µA	-40°C	V_{DD} = 3.3V (Sleep mode) Regulator Enabled
		0.23	**9**	µA	+25°C	
		0.32	**10**	µA	+60°C	
		0.51	**11**	µA	+85°C	
		5	**18**	µA	+125°C	
	PIC18FXXK80	0.22	**10**	µA	-40°C	V_{DD} = 5.5V(5) (Sleep mode) Regulator Enabled
		0.24	**10**	µA	+25°C	
		0.34	**11**	µA	+60°C	
		0.54	**12**	µA	+85°C	
		5	**20**	µA	+125°C	

Notes:

1. The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the device in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS}, and all features that add delta current disabled (such as WDT, SOSC oscillator, BOR, etc.).
2. The supply current is mainly a function of operating voltage, frequency, and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

   The test conditions for all IDD measurements in active operation mode are:

   - OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD};
   - $\overline{MCLR}$ = V_{DD}; WDT enabled/disabled as specified.
3. Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.
4. For LF devices, $\overline{RETEN}$ = 1.
5. For F devices, SRETEN = 1 and $\overline{RETEN}$ = 0.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X							

1.7. Module: Resets

1.7.1. An Unexpected Reset May Occur if the BOR Module is Disabled and Then Re-Enabled When the HLVD Module is Not Enabled

An unexpected Reset may occur if the Brown-out Reset (BOR) module is disabled, and then re-enabled, when the High/Low-Voltage Detection (HLVD) module is not enabled (HLVDCON[4] = `0`). This issue affects BOR modes:

- BOREN[1:0] = `'b10`
- BOREN[1:0] = `'b01`

In both of these modes, if the BOR module is re-enabled while the device is active, unexpected Resets may be generated.

Work around

If BOR is required and power consumption is not an issue, set BOREN[1:0] = `'b11`. For the BOREN[1:0] = `'b10` mode, either switch to the BOREN[1:0] = `'b11` mode or enable the HLVD module prior to entering Sleep mode.

If power consumption is an issue and low power is desired, do not use the BOREN[1:0] = `'b10` mode. Instead, use the BOREN[1:0] = `'b01` mode and follow the steps below when entering and exiting Sleep mode:

1. Disable the BOR by clearing SBOREN.
```
WDTCONbits.SBOREN = 0;
```
2. Enter Sleep mode (if desired).
```
SLEEP();
```
3. After exiting Sleep mode (if entered), enable the HLVD module.
```
HLVDCONbits.HLVDEN = 1;
```
4. Wait for the internal reference voltage (T_{IRVST}) to stabilize (typically 25 µs).
```
while(!HLVDCONbits.IRVST);
```
5. Re-enable the BOR by setting SBOREN.
```
WDTCONbits.SBOREN = 1;
```
6. Disable the HLVD module by clearing HLVDEN.
```
HLVDCONbits.HLVDEN = 0;
```

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.7.2. The $\overline{\text{MCLR}}$ Pin Will Not Be Readable When MCLRE = 0 for All 28-Pin Variants

The Master Clear pin will not be readable when MCLRE bit of CONFIG3H is set to off (MCLRE = 0) for all 28-pin device variants (PIC18(L)F2XK80). When the MCLRE bit is cleared on the 28-pin devices, the $\overline{\text{MCLR}}$ pin will be disabled but input data will not be available on RE3.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.8. Module: Timer1/3

1.8.1. Timer1/3 Gate Control Will Not Function Up to the Speed of F_{OSC} When TxCON is Set to the System Clock

Timer1 and Timer3 gate control will not function up to the speed of FOSC when the TxCON is set to the system clock (TxCON[7:6] = 'b01). Results will always be at the resolution of $F_{OSC}/4$, although the internal F_{OSC} has been selected as the clock source.

Work around

Use the external clock input pin setting, TxCON[7:6] = 'b10 and TxCON[3] = 0.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X						

1.8.2. Unexpected Interrupt Flag Generation May Occur in Asynchronous External Input Mode

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in the example below:

Example 1-1. Asynchronous Timer Mode Work Around to Avoid Spurious Interrupts

```
// Timer1 update procedure in Asynchronous mode
// The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;  // Stop timer from incrementing
```

```
PIE1bits.TMR1IE = 0;   // Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;          // Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;  // Turn on timer

/* Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1
interrupts. Depending upon clock edge timing relative to TMR1H/TMR1L
firmware write operation,a spurious TMR1IF flag event may sometimes assert.
If this happens, to suppress the actual interrupt vectoring, the TMR1IE bit
should be kept clear until after the "window of opportunity"(for spurious
interrupt event has passed). After the window is passed, no further
spurious interrupts occur, at least until the next timer write
(or mode switch/enable event).*/

while(TMR1L < 0x02);  // Wait for 2 timer increments more than the updated
                      // timer value (indicating more than 2 full T1CKI
                      // clock periods elapsed)
NOP();                // Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;  // Clear TMR1IF in case it was spuriously set
PIE1bits.TMR1IE = 1;  // Re-enable interrupt vectoring for Timer1
```

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

1.9. Module: Primary Oscillator

1.9.1. XT Primary Oscillator Mode Does Not Reliably Function When the Driving Crystals are Above 3 MHz

On some devices, using the XT oscillator at the top end of its specified frequency range (3.0 - 4.0 MHz) may cause the device to cease driving the oscillator.

Work around

Use the XT mode only for frequencies lower than 3.0 MHz.

Use the HS mode if frequencies greater than 4.0 MHz on a crystal oscillator are required.

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X					

1.10. Module: Instruction Set

1.10.1. The `PUSHL` Instruction Incorrectly Executes

The `PUSHL` instruction of the PIC18 Extended Instruction Set incorrectly executes when FSR2 is loaded with certain values.

Work around

Do not use `PUSHL` when FSR2 is loaded with any of the following values:

- 0xDB
- 0xDC
- 0xDE
- 0xE3
- 0xE4
- 0xE6
- 0xEB

- 0xEC
- 0xEE

Affected Silicon Revisions

A2	A3	A4	A6	**A7**			
X	X	X	X	**X**			

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30009977**G**):

Note:
Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1. ADCON2 (Register 23-3)

Register 23-3 (ADCON2) is missing Note 2 pertaining to the configuration of the A/D Acquisition Time Selection bits. The updated register notes are shown below with Note 2 highlighted in **bold**:

Notes:

1. If the A/D FRC clock source is selected, a delay of one T_{CY} (instruction cycle) is added before the A/D clock starts. This allows the `SLEEP` instruction to be executed before starting a conversion.
2. **When ACQT[2:0] = `'b000`, ADC saturation may occur due to the short period of discharge time. Use ACQT[2:0] != `'b000` to improve this situation for accurate measurement.**

3. Appendix A: Revision History

Doc Rev.	Date	Comments
R	04/2025	Updated the document format to the current Microchip publication standard, module numbers under silicon errata have been renumbered accordingly. Added silicon revision A7; added silicon issue 1.10.1.
Q	05/2023	Added DS Clarification 1.
P	06/2018	Added silicon issue 15.
N	11/2017	Removed all DS Clarifications.
M	07/2017	Added DS Clarification 12.
L	01/2017	Added DS Clarification 11; other minor corrections.
K	04/2016	Added silicon issues 13 and 14; added DS Clarifications 9 and 10; other minor corrections.
J	07/2015	Removed DS Clarifications 1-6, renumbered remaining issues.
H	07/2014	Added silicon issue 11.
G	04/2014	Added DS Clarification 11; other minor corrections.
F	02/2014	Added silicon revision A6; added DS Clarifications 9 and 10; other minor corrections.
E	12/2013	Added MPLAB X IDE; updated silicon issue 1; added silicon issue 11; added DS Clarifications 7 and 8; other minor corrections.
D	12/2011	Added silicon revision A4; updated DS revision to 'D' ; added DS Clarification 6.
C	09/2011	Added Table 3 to silicon issue 1, added silicon issues 9 and 10; added DS Clarifications 4 and 5.
B	04/2011	Added silicon issues 7 and 8; added DS Clarifications 1, 2, and 3.
A	02/2011	Initial release of this document.

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