MOS RAMs

MM2101, MM2101-1, MM2101-2 1024-bit (256 × 4) static MOS RAM with separate I/O

general description

The National MM2101 is a 256 word by 4 bit static random access memory element fabricated using N-Channel enhancement mode Silicon Gate technology. Static storage cells eliminate the need for refresh and the additional peripheral circuitry associated with refresh. The data is read out nondestructively and has the same polarity as the input data.

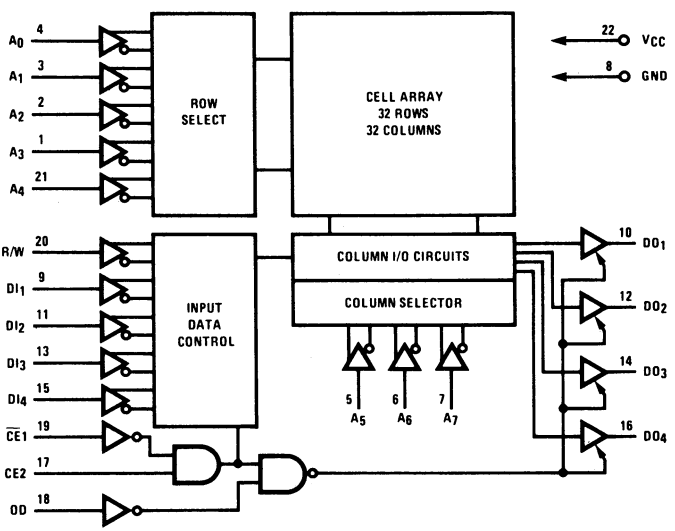
The 2101 is directly TTL compatible in all respects: inputs, outputs, and a single +5 V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The features of this memory device can be combined to make a low cost, high performance, and easy to manufacture memory system.

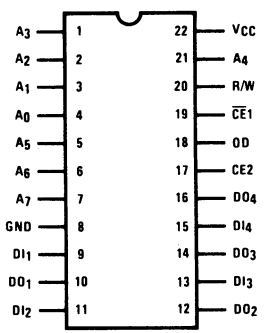
National's silicon gate technology also provides protection against contamination, and permits the use of low cost Epoxy B packaging.

features

- Organization 256 Words by 4 Bits
- Access Time – 0.5 to 1.0 μs Max.
- Single +5 V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Chip Enable Input
- Low Cost Packaging – 22 Pin Epoxy B Dual-In-Line Configuration
- Low Power – Typically 150 mW
- Tri-State ® Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

block and connection diagrams





PIN NAMES

$DI_1 - DI_4$	DATA INPUT
$A_0 - A_7$	ADDRESS INPUTS
R/W	READ/WRITE INPUT
CE1, CE2	CHIP ENABLE
OD	OUTPUT DISABLE
$DO_1 - DO_4$	DATA OUTPUT
V_{CC}	POWER (+5 V)

Order Number MM2101D, MM2101-1D or MM2101-2D
See Package 5

Order Number MM2101-N, MM2101-1N or MM2101-2N
See Package 17

absolute maximum ratings

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5 V to +7 V
Power Dissipation	1 Watt

dc electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified.

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Current			10	μA	$V_{IN} = 0$ to 5.25 V
I_{LOH}	I/O Leakage Current[2]			15	μA	$\overline{CE}1 = 2.2\ V$, $V_{OUT} = 4.0\ V$
I_{LOL}	I/O Leakage Current[2]			-50	μA	$\overline{CE}1 = 2.2\ V$, $V_{OUT} = 0.45\ V$
I_{CC1}	Power Supply Current		30	60	mA	$V_{IN} = 5.25\ V$, $I_O = 0\ mA$, $T_A = 25°C$
I_{CC2}	Power Supply Current			70	mA	$V_{IN} = 5.25\ V$, $I_O = 0\ mA$, $T_A = 0°C$
V_{IL}	Input "Low" Voltage	-0.5		+0.65	V	
V_{IH}	Input "High" Voltage	2.2		V_{CC}	V	
V_{OL}	Output "Low" Voltage			+0.45	V	$I_{OL} = 2.0\ mA$
V_{OH}	Output "High" Voltage	2.2			V	$I_{OH} = -150\ \mu A$

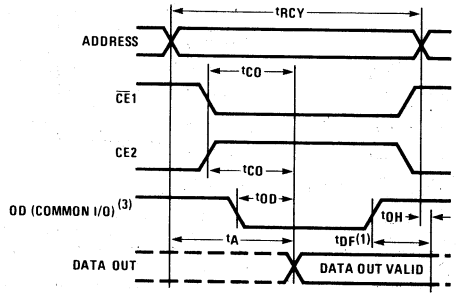
Note 1: Typical values are for $T_A = 25°C$ and nominal supply voltage.
Note 2: Input and Output tied together.

capacitance $T_A = 25°C$, f = 1 MHz

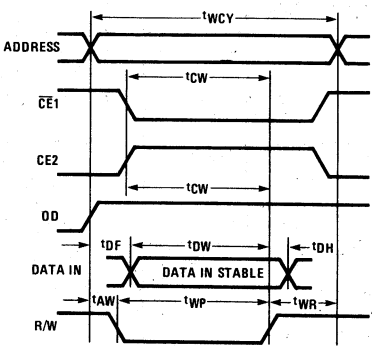
Symbol	Test	Limits (pF)	
		Typ.	Max.
C_{IN}	Input Capacitance (All Input Pins) $V_{IN} = 0\ V$	4	8
C_{OUT}	Output Capacitance $V_{OUT} = 0\ V$	8	12

switching time waveforms

READ CYCLE (R/W = "1")



WRITE CYCLE[2]



Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE}1$, CE2, or OD, whichever occurs first.
Note 2: During the write cycle, OD is a logical 1 for common I/O and "don't care" for separate I/O operation.
Note 3: OD should be tied low for separate I/O operation.

ac electrical characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5\ V \pm 5\%$, unless otherwise specified.

MM2101

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			1,000	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			800	ns	20 ns
t_{OD}	Output Disable to Output			700	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		200	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
WRITE CYCLE						
t_{WCY}	Write Cycle	1,000			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	900			ns	20 ns
t_{DW}	Data Setup	700			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	750			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	$C_L = 100\ pF$

MM2101-1 (500 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	500			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			500	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			350	ns	20 ns
t_{OD}	Output Disable to Output			300	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		150	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
WRITE CYCLE						
t_{WCY}	Write Cycle	500			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	100			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	400			ns	20 ns
t_{DW}	Data Setup	280			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	300			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	$C_L = 100\ pF$

MM2101-2 (650 ns Access Time)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
READ CYCLE						
t_{RCY}	Read Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_A	Access Time			650	ns	Input Pulse Rise and Fall Times:
t_{CO}	Chip Enable to Output			400	ns	20 ns
t_{OD}	Output Disable to Output			350	ns	Timing Measurement Reference
t_{DF}[1]	Data Output to High Z State	0		150	ns	Level: 1.5 V
t_{OH}	Previous Data Read Valid after change of Address	0			ns	Output Load: 1 TTL Gate and $C_L = 100\ pF$
WRITE CYCLE						
t_{WCY}	Write Cycle	650			ns	Input Pulse Levels: +0.65 to +2.2 V
t_{AW}	Write Delay	150			ns	Input Pulse Rise and Fall Times:
t_{CW}	Chip Enable to Write	550			ns	20 ns
t_{DW}	Data Setup	400			ns	Timing Measurement Reference
t_{DH}	Data Hold	100			ns	Level: 1.5 V
t_{WP}	Write Pulse	400			ns	Output Load: 1 TTL Gate and
t_{WR}	Write Recovery	50			ns	$C_L = 100\ pF$

Note 1: t_{DF} is with respect to the trailing edge of $\overline{CE}1$, CE2, or OD, whichever occurs first.