Section 1: SmartNixie Overview

The TES SmartNixie is a family of self contained I^2C addressable nixie modules. With the on board 4 position DIP switch the I^2C slaves may be set for addresses from 0x10 to 0x1E (8 slaves) or the lower address inputs A_0 and A_1 can be configured to be read as analog inputs. In the analog input mode, slave addresses can range from 0x10 to 0xEE (112 slaves) where addresses 0x10 to 0x1E are the same as for the digital input mode. So long as the resistor dividers that set the analog address operate from the same Vdd as the module, only the resistor tolerance is a factor in the accuracy of the internal address computation.

The first eight analog device addresses put the SmartNixie module into one of eight special operating modes, e.g. Mode 5 is "Ripple counter" where modules can be connected as shown in Figure 8 to build counter chains of any length. See Table 3 for the complete special mode list.

When the A_3/A_2 address inputs are set to 1/1, the SmartNixie module operates as a master I^2C device, controlling five other slave modules to create one of two simple six digit clock designs. Figure 12 illustrates the simplest version which uses an external 50/60Hz line reference for time keeping showing time in a HH:MM:SS format. Figure 13 illustrates a slightly more complex configuration which uses a stand alone Real Time Clock IC and on board back up battery for nearly 1 year of unpowered timekeeping as well as a perpetual calendar function. For the ultimate in clock accuracy, a GPS RTC module is available which has an RS232 port with NMEA output.

The SmartNixie modules operate from a Vdd of 2.0 to 5.5VDC and communicate on the I^2C bus at 100Kbps. Typical supply current into Vdd is < 2.5mA at 5.5VDC. The nixie anode supply is typically 170V and the cathode drivers are rated for 240V and 100mA of sink current with only 100nA of off current at 240VDC.

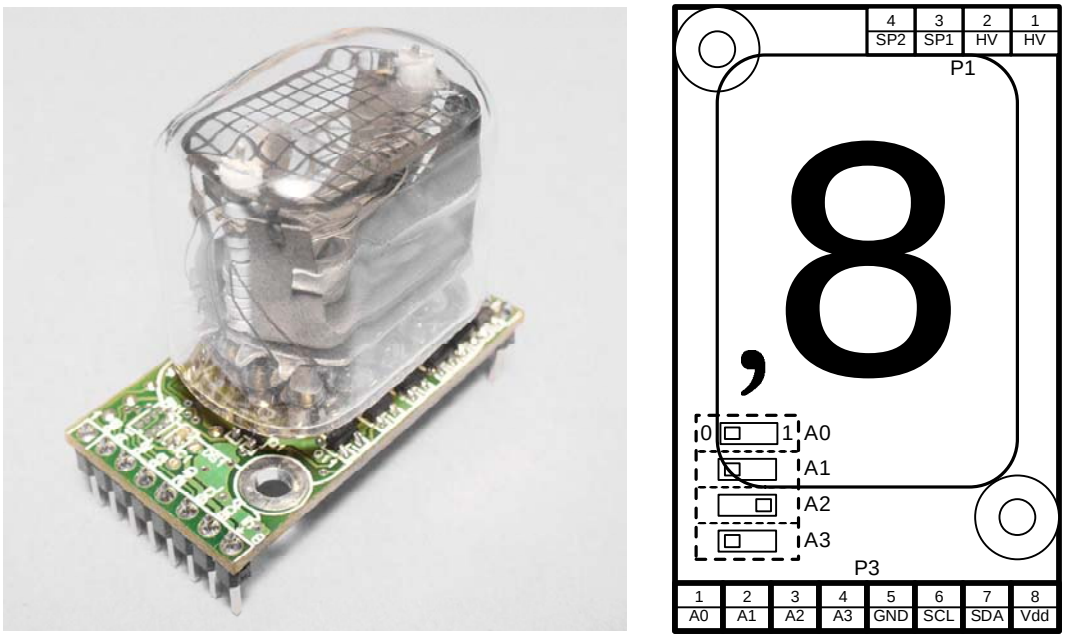


Figure 1: SmartNixie (IN12 module shown)

Revision History

Date	FW	Affects	Description
2007/10/02	All	All	Initial release.
2008/04/27	01.02	Table 4	Changed setting entry delay from 5 to 2 seconds.
2009/02/11	N/A	Fig 8	Change reset resistor from 10K to 1K to overcome multiple module pull ups, should be >300uA per module in parallel.
	01.04	Table 3	Added Nixie/Numitron modes.
	01.04	Table 4	Added Nixie/numitron selection and new 12/24 hour display selections.
	01.04	Table 4	Added trim forward and back to adjust for slow and fast clocks.
2009/05/01	01.06	Table 4	Note 1 now indicates right 2 digits blank during setting. Older firmware blanked center 2 digits which did not work for 4 digit clocks.
	N/A	Fig 12/13	Updated to show typical HVPS and RTC module numbers.
	N/A	Fig 21	Removed schematic and replaced it with the IN4 mechanical outline as well as added IN18 and module outlines at end of document.
2009/11/01	01.07	Table 4	Added colon control to clock setting menus.
		Table 4	Moved Table 4 notes to next page for table expansion.
		Fig 12/13	Added colon connections.
2009/12/21	N/A	Overview	Change RTC backup time from ">2 years" to "Up to 1 year".
	N/A	All	Change Vdd range to 2.0 to 5.5V; the RTC lower limit is 3.0 for battery charging which sets the system lower limit when the RTC is used. The GPS RTC lower limit is 3.5V when RS232 is not used and 5.0V when RS232 is used to read NMEA messages with a PC.
2010/06/27	01.07	Table 5	Updated command register to match firmware (Was 0-3 and 0x96, now 1-4 and 0xF0) and added address pin read command 0xF1. Register 0x00 now shows write and read modes.

Table 1a: Interface connector signals, horizontal modules (IN4, IN12 and IN18)

Pin		Name	Description
P1	1	HV	+170V nixie anode voltage
	2	HV	Connected to pin 2
	3	Spare1	Aux cathode / IN12B comma
	4	Spare2	Aux cathode / Colon driver
P3	1	A0	Address 0 of module[1]
	2	A1	Address 1 of module[1]
	3	A2	Address 2 of module[2]
	4	A3	Address 3 of module[3]
	5	GND	Power input, 0V
	6	SCL	I^2C serial clock (I^2C Mode)
	7	SDA	I^2C serial data (I^2C Mode)
	8	Vdd	Power input, 2.0V-5.5V

Table 1b: Interface connector signals, vertical module (INxx)

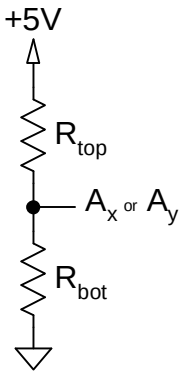
Pin		Name	Description
P1	1	A0	Address 0 of module[1]
	2	A1	Address 1 of module[1]
	3	A2	Address 2 of module[2]
	4	A3	Address 3 of module[3]
	5	SCL	I^2C serial clock (I^2C Mode)
	6	SDA	I^2C serial data (I^2C Mode)
	7	GND	Power input, 0V
	8	Vdd	Power input, 2.0V-5.5V
	9	Spare2	Aux cathode / Colon driver
	10	GND	Power input, 0V
	11	Spare1	Aux cathode / IN12B comma
	12	HV	+170V nixie anode voltage

Notes:
1. When A1/A0 are 0/0, 0/1 or 1/1 these pins are configured as digital inputs pulled up to Vdd with a 50-450uA current. When A1/A0 are 1/0 these pins are configured as analog inputs with no pull ups.
2. A2 is always pulled up to Vdd with 100K.
3. A3 is always pulled up to Vdd with a 50-450uA current.

Section 2: SmartNixie Addressing

Table 2: Module Addressing

DIP Switch					
A_3	A_2	A_1	A_0	Base Addr	Description
0	0	0	0	**0x10**	Simple slave addressing, DIP switch is read as digital input with pull ups active.
0	0	0	1	**0x12**	
0	0	1	0	**0x14**	
0	0	1	1	**0x16**	
0	1	0	0	**0x18**	
0	1	0	1	**0x1A**	
0	1	1	0	**0x1C**	
0	1	1	1	**0x1E**	
1	0	0	A_y		See Table 3 for special modes
1	0	A_x	A_y	**0x10-0xEE**	Extended slave addressing...



Rx Values
6.19K-1%
10.0K-1%
13.3K-1%
15.0K-1%
38.3K-1%
130K-1%

Ax and Ay are configured as analog inputs without pull-ups in this mode, where the unit base address can be computed from...

$(((Bin_{Ax} \times 11) + Bin_{Ay}) \times 2) - 2$

...yielding 112 unique slave base addresses ranging from **0x10** to **0xEE**.

The Voltage Bins are defined as follows with example resistor divider values shown such that only 6 different 1% values are required:

Bin	Voltage	Rtop	Rbot	Rtot	I-uA
0	0.227	130K	6.19K	136K	37
1	0.682	38.3K	6.19K	44.5K	112
2	1.136	130K	38.3K	168K	30
3	1.591	13.3K	6.19K	19.5K	256
4	2.045	15.0K	10.0K	25.0K	200
5	2.500	38.3K	38.3K	76.6K	65
6	2.955	10.0K	15.0K	25.0K	200
7	3.409	6.19K	13.3K	19.5K	256
8	3.864	38.3K	130K	168K	30
9	4.318	6.19K	38.3K	44.5K	112
10	4.773	6.19K	130K	136K	37

The A/D conversion is 10 bits so that the above values give better than +/-30 counts of margin beyond the resistor tolerance limits.

1	1	m	m		Clock modes, see Table 3

Notes:
1. Voltage bins shown are based on 5V into Vdd but are actually ratiometric such that the same divider resistors will yield the same address/mode for any Vdd within the allowed operating range.

Section 2: SmartNixie Addressing

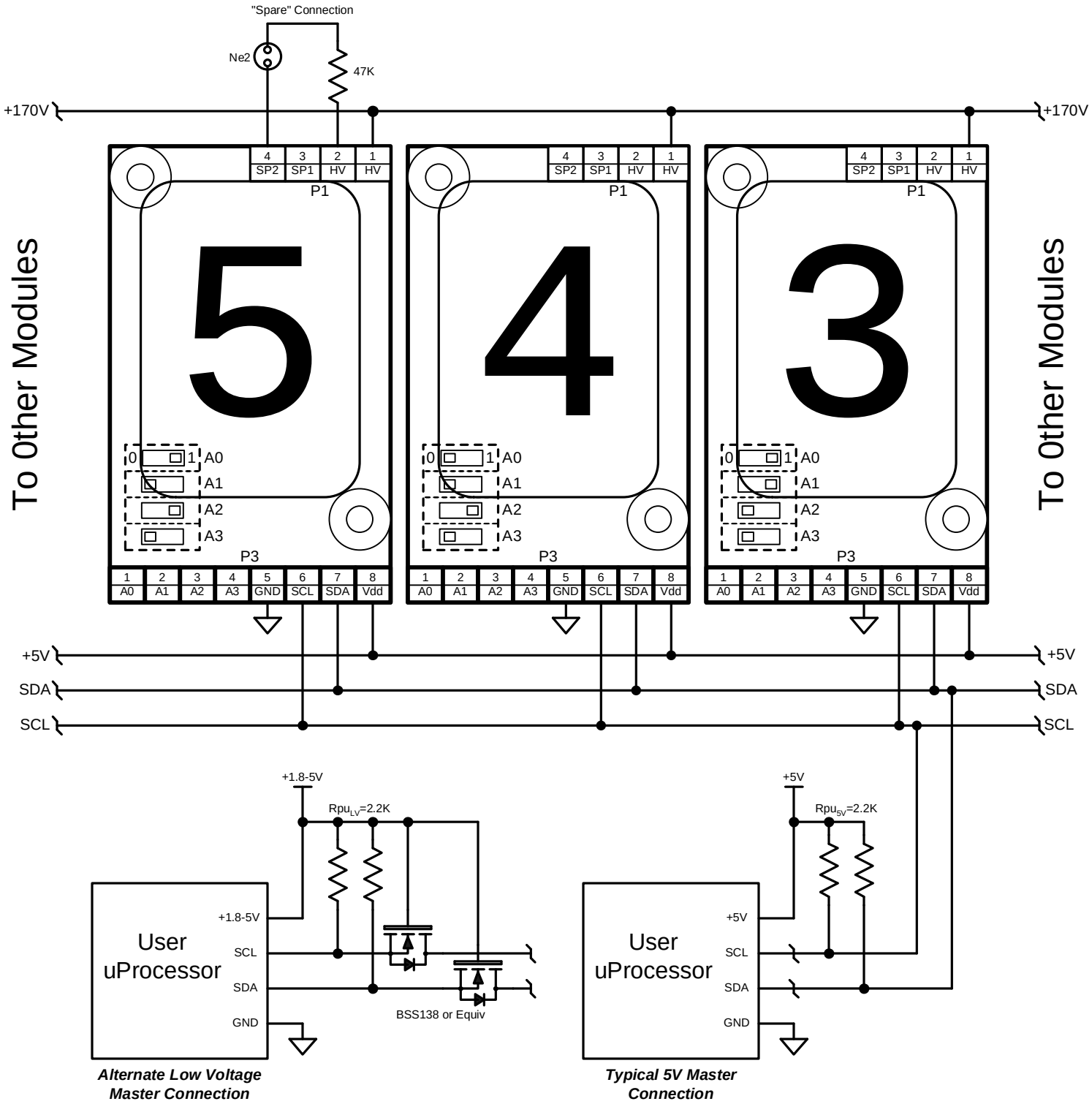
Table 3: Module Addressing, Special Modes

DIP Switch				A_y Value			
A_3	A_2	A_1	A_0	Bin	Volts	Mode	Special Mode Description: I^2C is disabled
1	0	0	A_y	0	0.227	**0**	Burn-in Nixie counter free running at 10Hz (Figure 3)
				1	0.682	**1**	Burn-in Numitron counter free running at 10Hz (Figure 3)
				2	1.136	**2**	Reserved for future use
				3	1.591	**3**	Reserved for future use
				4	2.045	**4**	Reserved for future use
				5	2.500	**5**	Ripple counting Nixie (Figure 8)
				6	2.955	**6**	Ripple counting Numitron (Figure 8)
				7	3.409	**7**	Reserved for future use
				8	3.864	**8**	Version/Serial# stream on SCL, Async 19.2Kbps (Figure 11)
				9	4.318	**0x10**	*Standard mode slave address = 0x10*
				10	4.773	**0x12**	*Standard mode slave address = 0x12*
1	1	0	x	---	---	**9**	6 digit clock master with 60Hz reference into A_0 (Figure 12)[3]
1	1	1	x	---	---	**10**	6 digit clock/calendar master using PCF8563 RTC (Figure 13)

Notes:

1. Voltage bins shown are based on 5V into Vdd but are actually ratiometric such that the same divider resistors will yield the same address/mode for any Vdd within the allowed operating range.
2. Reserved mode addresses operate as the Burn-in counter mode when selected.
3. The default line frequency is 60Hz but 50, 60 and 100Hz line clock dividers are selectable via the clock setting controls.

Section 3: SmartNixie Applications

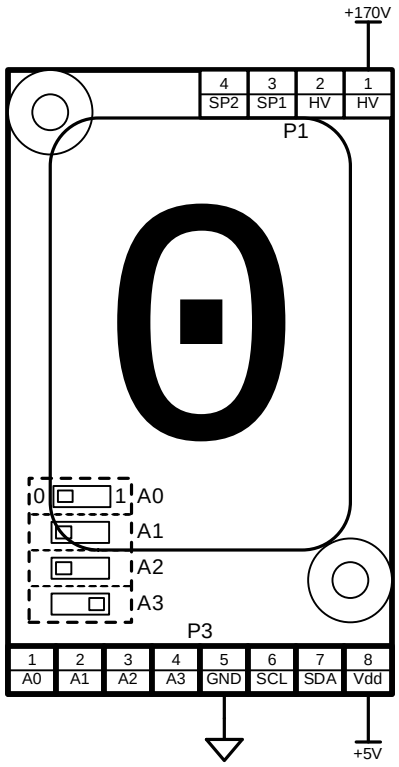


Alternate Low Voltage Master Connection

Typical 5V Master Connection

Figure 2: Typical Slave Bus Connection (Addr=0x10 to 0xEE)

Section 3: SmartNixie Applications



Unit will count 0-9 at
about a 10Hz rate

Figure 3: Stand Alone Burn-in Counter (Mode=0)

Section 3: SmartNixie Applications

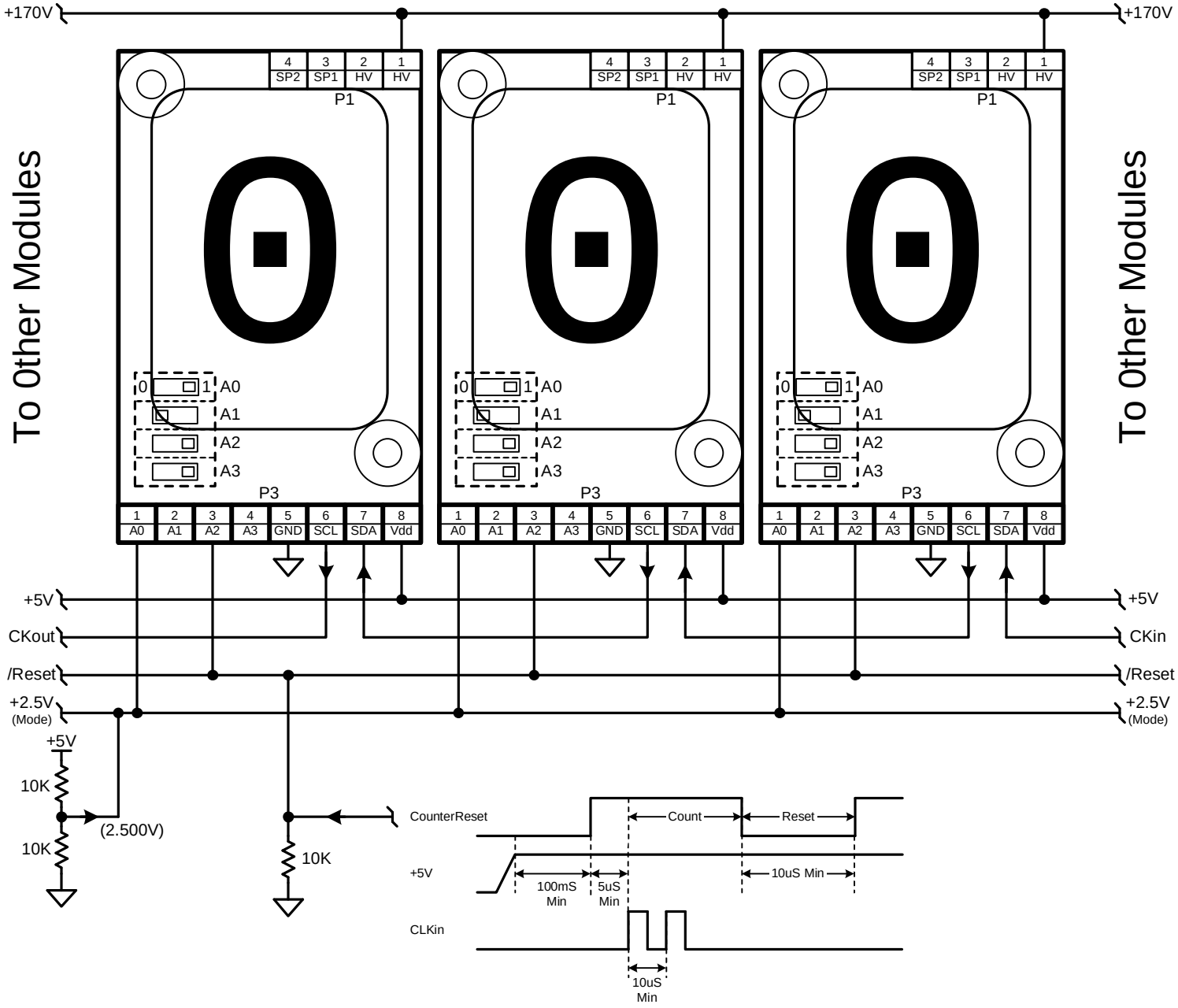


Figure 8: Ripple Counter Mode Connection, No Dimming (Mode=5)

Section 3: SmartNixie Applications

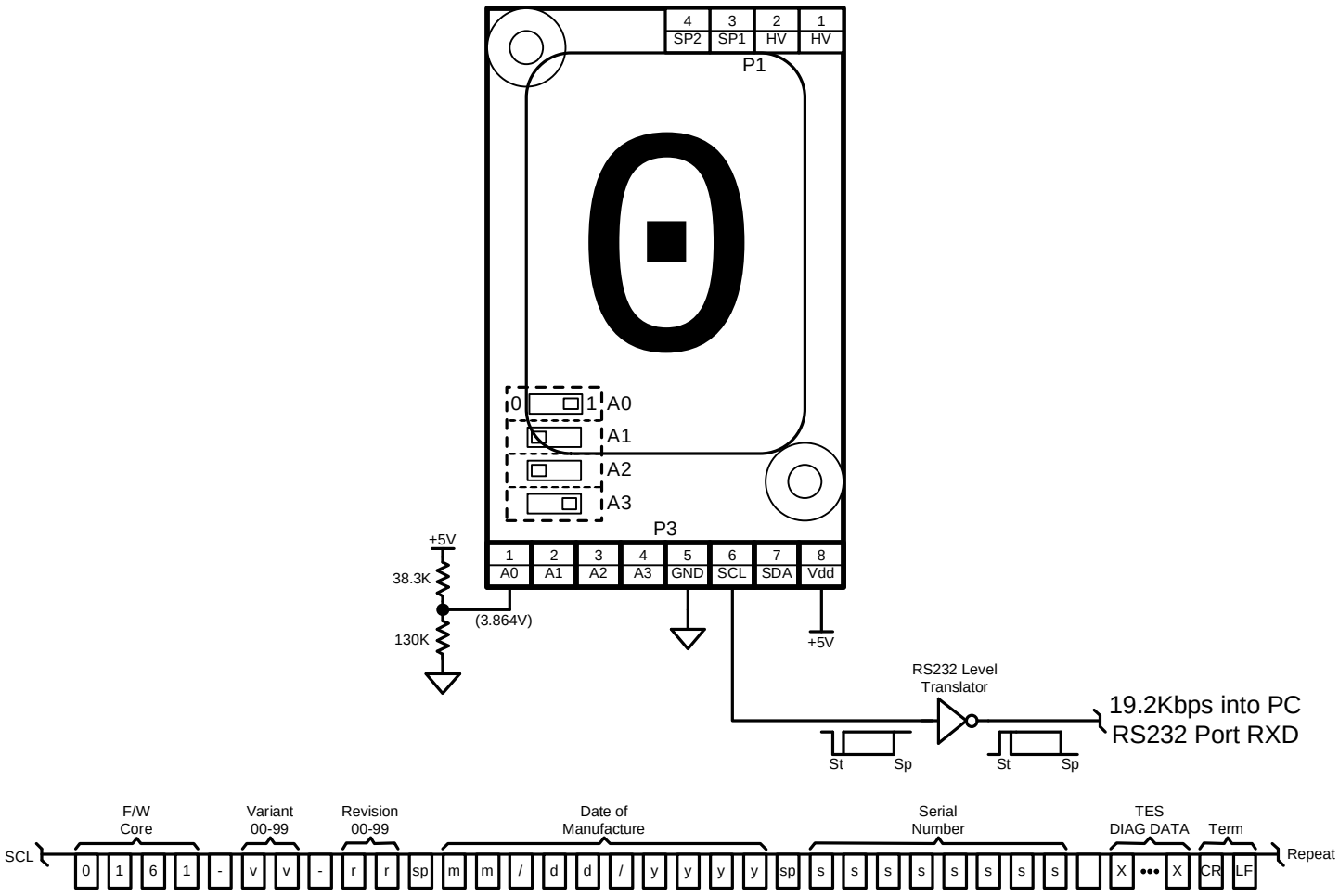


Figure 11: Serial Number / Version Data Stream (Mode=8)

Section 3: SmartNixie Applications

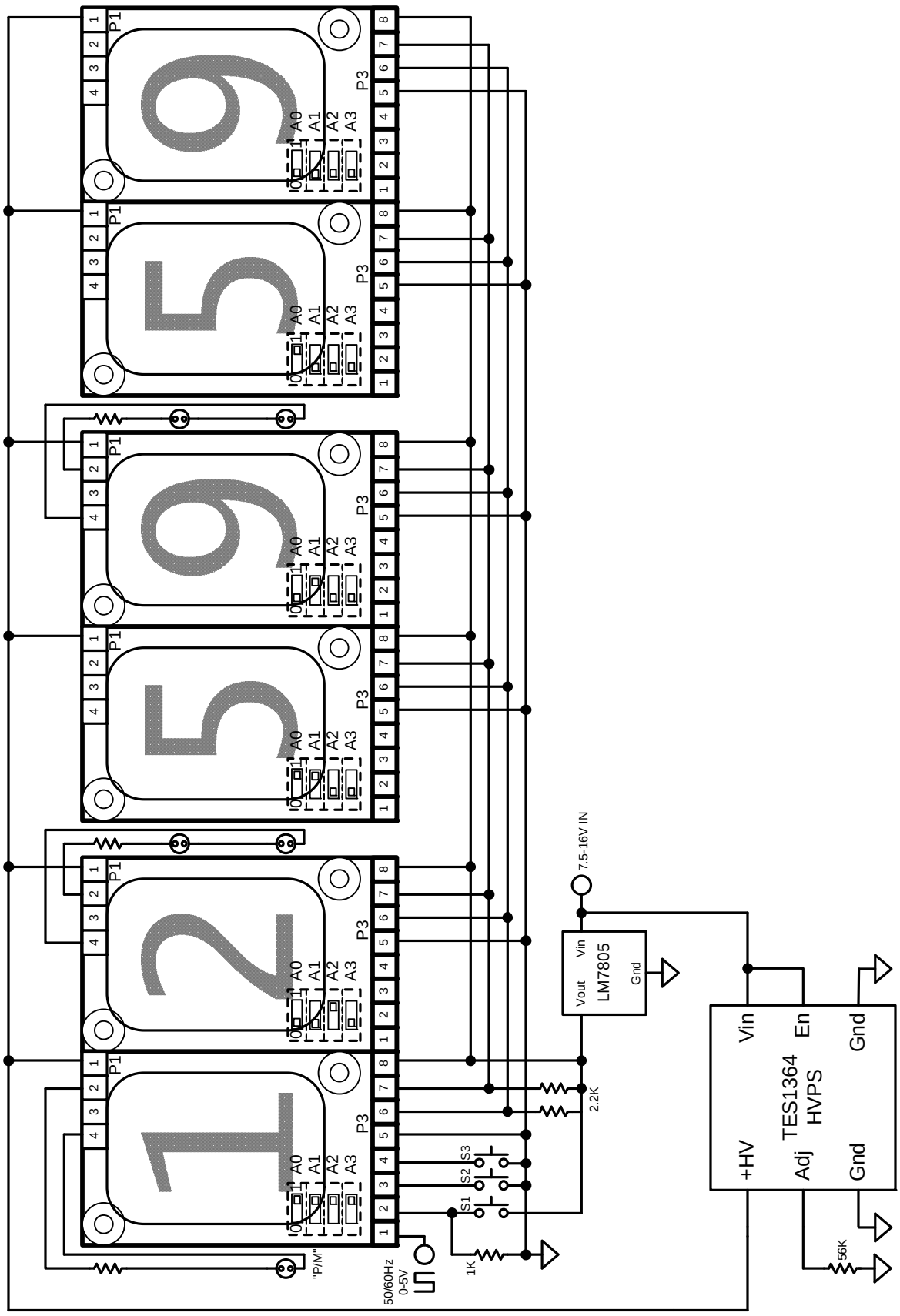


Figure 12: Typical Application, 60Hz Reference Clock (Mode=9)

Section 3: SmartNixie Applications

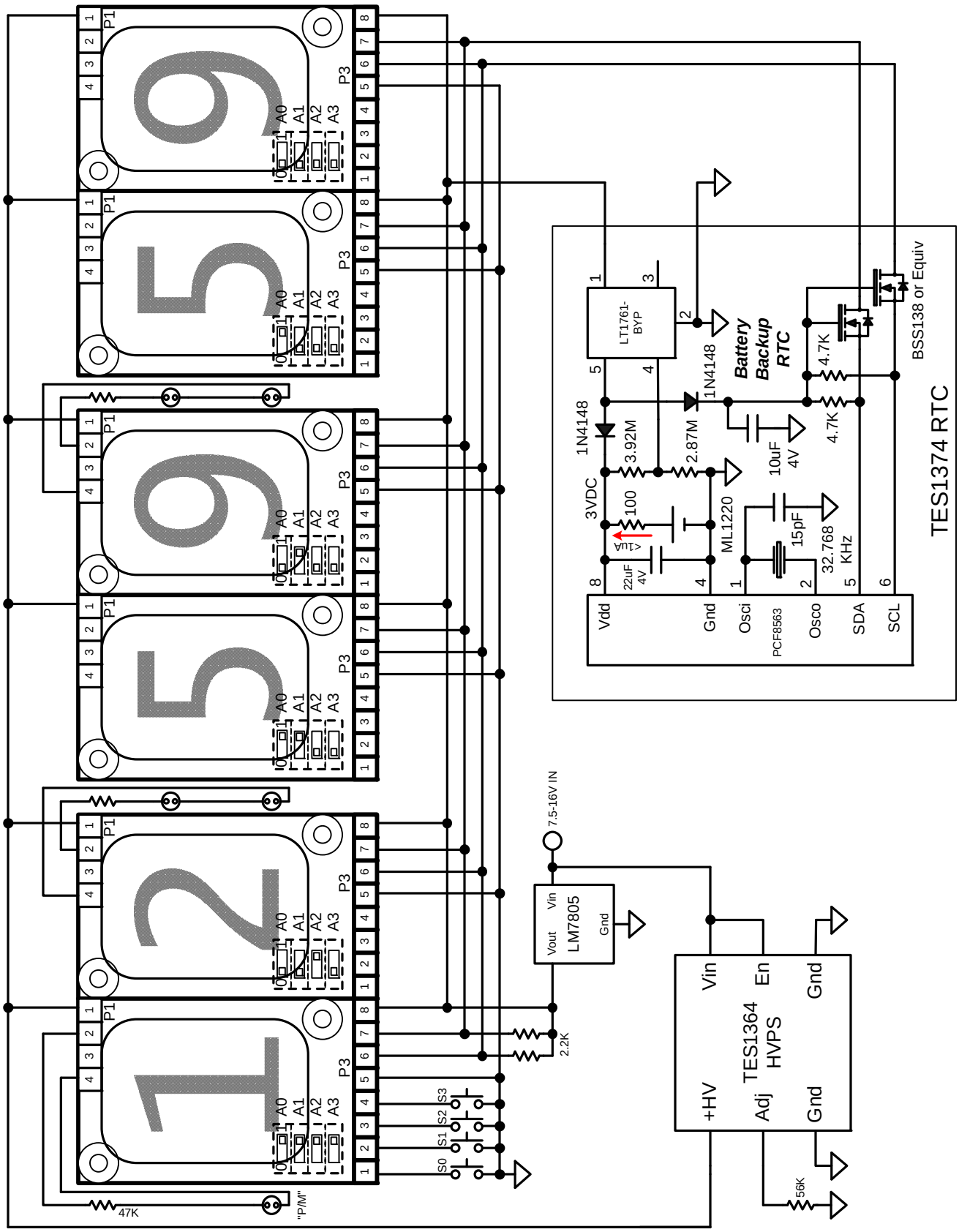


Figure 13: Typical Application, Stand Alone Clock/Calendar (Mode=10)

Section 3: SmartNixie Applications

Table 4: Clock setting (Modes 9 and 10), FW 0161.01.07

Button Press				Function Description
S3	S2	S1	S0	
			X	Show the date in the format MM:DD:YY (Only available in RTC clock Mode 10)
	X	X		Hold for >2 seconds to switch between Nixie and Numitron display modes
X	X			Hold for >2 seconds to increment the current time by 1 second: Adjusts for slow clock
X		X		Hold for >2 seconds to decrement the current time by 1 second: Adjusts for fast clock
X				Hold for >2 seconds to enter setting mode
X				While in setting mode, press >150mS and <2 seconds to advance to next setting selection

Display						
Mode	Mode	10's	1's	---	---	Function
0	0	H	H	---	---	Hours [1]
0	1	M	M	---	---	Minutes
0	2	S	S	---	---	Seconds
0	3	Mo	Mo	---	---	Mode 10: Months
0	4	D	D	---	---	Mode 10: Days
0	5	Y	Y	---	---	Mode 10: Years
0	6	C	C	---	---	12/24 hour clock display select (S1 and S2 steps through selections)
		0	1			12 hour mode, leading hours 10's zero displayed
		1	2			12 hour mode, leading hours 10's zero blanked
		0	2			24 hour mode, leading hours 10's zero displayed
		2	4			24 hour mode, leading hours 10's zero blanked
0	7	L	L	---	---	Mode 9: Line frequency select (S1 and S2 steps through selections)
		0	0			No prescale, free-run clock
		0	1			Divide-by-1
		1	0			Divide-by-10
		5	0			Divide-by-50
		6	0			Divide-by-60
		5	2			Divide-by-100 (50 x 2)
		6	2			Divide-by-120 (60 x 2)
		9	9			Divide-by-255
0	8	8	8	---	---	Dimmer setting, 10-100% [2]
0	9	M	M	---	---	Colon display mode [6]
		0	0			Off
		0	1			On
		0	2			Blinking at 0.5 Hz: On 1 second / Off 1 second

X				Hold for >2 seconds to exit setting mode, executes upon release [3/4]
	X			While in the setting mode, advances the 10's digit, 150mS auto increment
		X		While in the setting mode, advances the 1's digit, 150mS auto increment

Mode 9 and 10 clock setting notes:

1. For the RTC clock (Mode 10), exiting the setting mode when the display shows "00 HH --" will only save the configuration data but the time will not be updated to the RTC module. For the line clock (Mode 9), time is updated regardless of the current setting menu since time is counted internally using the same registers used to display the new settings.

2. "88" is displayed at the current dimming selection while the mode display remains at 100% brightness. In this mode, S2 increases and S1 decreases the brightness level in 5% steps. Upon exiting the setting mode the entire display is set to the newly selected brightness level once S3 is released.

3. To align the clock time with an external reference: Set the time ahead and then press and hold S3 down for more than 2 seconds to exit the setting mode at any position other than "00" per note 1 which will display the newly set time. When the advancing reference time matches the clock display, release S3 to resume normal time counting.

4. The Nixie/Numitron, 12/24 hour display, Line frequency, Colon control and Dimmer selection settings are stored in EEPROM upon exiting the setting mode so that they can be restored when the power is cycled.

5. For the GPS RTC module, after the GPS fix is acquired and time starts counting normally, adjust the clock to the current local time to allow the module to store and the automatically compute your local time zone offset.

6. Neon bulbs may be connected to the Hours-1s and Minutes-1s display modules to allow software control of colon indicators. On the backplanes the anodes of the colons are connected to E4 and E10 through current limiting resistors and the cathodes are connected to E6 and E12. When a backplane is not used, the anodes are connected to the "HV" signal through current limiting resistors and the cathodes are connected to the "SP2" signals: See individual module schematics to locate these signals.

Section 4: SmartNixie Communication

An I²C master communicates with groups of TES1328 modules configured as slaves via a sixteen element register stack using standard I²C commands at a maximum data rate of 100kbps. See Table 5 for a complete list of the slave stack register functions.

For register writes a Start command is issued followed by the slave address where the R/W bit is cleared to zero. The next byte written is the pointer to the desired element in the register stack from 0x00 to 0x0D where this pointer is automatically trimmed to the four LSBs. The next bytes written are the register data and after the last register data byte has been sent, a Stop command is issued which completes the transaction. Each write by the master is followed by a low ACK bit generated by the slave indicating an acknowledgement of the transaction, where a high NAK bit generally indicates no slave at the specified address is present.

After each write the internal register pointer is incremented allowing from one to fourteen consecutive registers to be written in the same transaction. Writes beyond the last writeable register position (0x0D) are ignored. Two byte registers are executed after the second (Low) byte has been received.

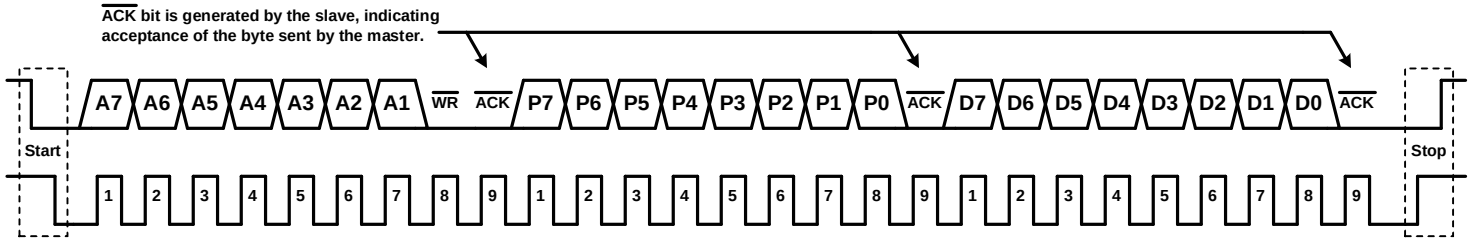


Figure 15: Typical Write Sequence

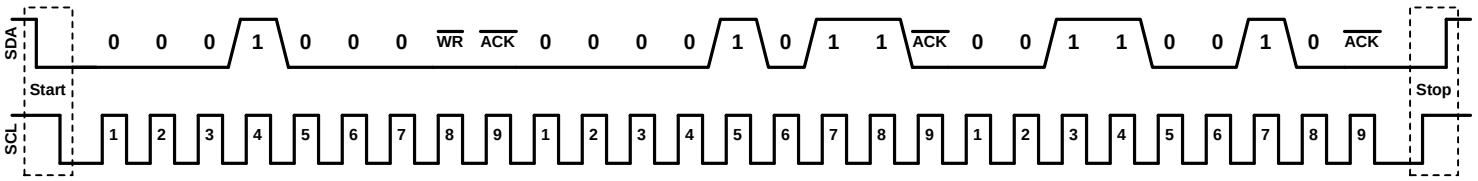


Figure 16a: Write to slave 0x10, Register 0x0B with Data 0x32 (50% dimmer)

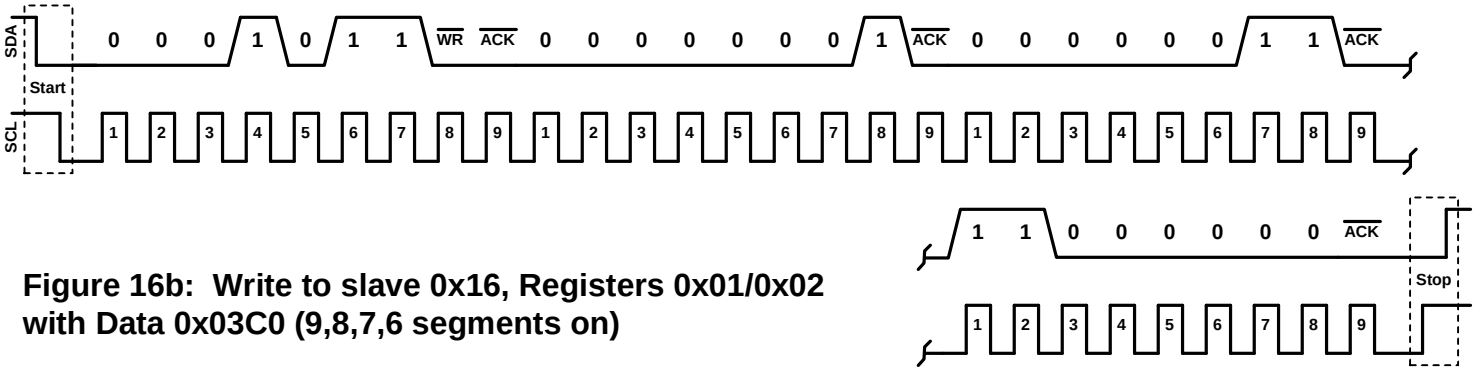


Figure 16b: Write to slave 0x16, Registers 0x01/0x02 with Data 0x03C0 (9,8,7,6 segments on)

Section 4: SmartNixie Communication

For register reads a Start command is issued followed by the slave address where the R/W bit is set to one. The first byte read is always register 0x00 and each additional read returns the next byte in the register stack from 0x01 to 0x0F where the internal pointer is automatically trimmed to the four LSBs so that the sixteenth byte read is register 0x00 and so on. After the last register has been read by the master, a Stop command is issued which completes the transaction. Each read by the master is followed by a low ACK bit generated by the master except for the last read which must be followed by a high NAK bit from the master signaling to the slave that no further bytes will be read.

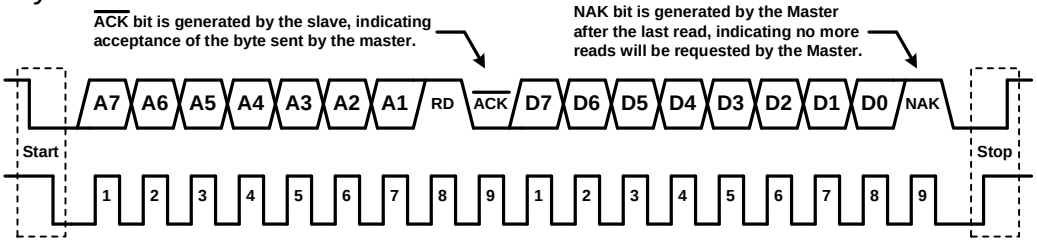


Figure 17: Typical One Byte Read Sequence

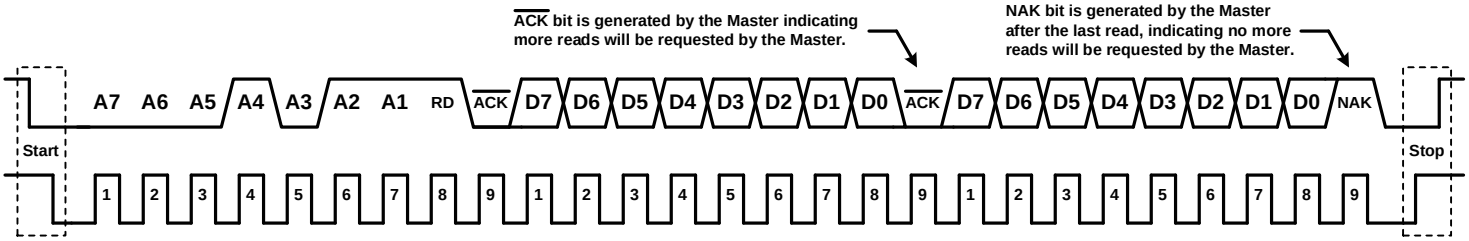


Figure 18a: Multi Byte Read Sequence from Slave 0x16

```
//PICC code for Figure 16a
I2C_START();
I2C_WRITE(0x10);        //slave address, R/W set low
I2C_WRITE(0x0B);        //register address=dimmer
I2C_WRITE(0x32);        //dimmer=50%
I2C_STOP();

//PICC code for Figure 16b
I2C_START();
I2C_WRITE(0x16);        //slave address, R/W set low
I2C_WRITE(0x01);        //register address=bitmap
I2C_WRITE(0x03);        //high byte, "9","8" on
I2C_WRITE(0xC0);        //low byte, "7","6" on
I2C_STOP();

//PICC code for Figure 18a
//Reads from slave always begin with register 0x00
I2C_START();
I2C_WRITE(0x17);        //slave address, R/W set high
data1=I2C_READ(0);      //reads register 0x00
data2=I2C_READ(1);      //reads register 0x01 (and so on)
I2C_STOP();             //  last read is always (1)=NAK
```

Figure 19: Example coding

Section 4: SmartNixie Communication

Table 5: Slave Mode Control Registers

Register	Name	Description
0x00 (Wr)	Character (Nixie) 7 6 5 4 3 2 1 0 S_2 S_1 x B n n n n	n...n 0x0-0xB displays "0"-"9", Spare1 and Spare2 0xC-0xF displays 3 segment test blocks B 1 Blanks and 0 enables the n...n display data S_2,S_1 Turns on the spare channels independently of the state of B and n...n bits
0x00 (Rd)	Read address pins 7 6 5 4 3 2 1 0 0 0 0 0 A_3 A_2 A_1 A_0	The state of the address pins are read and then stored here after 0xF0 is written to register 0x0D. The result may then be retrieved at the next I^2C read transaction.
0x01 0x02 (Wr)	BitmapHigh BitmapLow	Any combination of segments can be enabled and are updated when the register BitmapLow is written. Bits marked "x" are don't care.
0x03 (Wr)	SevenSeg (Numitron) 7 6 5 4 3 2 1 0 S_2 S_1 Dp B n n n n	n...n 0x0-0xF displays "0"-"9", "A"-"F" B 1 Blanks and 0 enables the n...n display data S_2,S_1,Dp Turns on the spare and decimal point channels independently of the state of B and n...n bits
0x04-0x05	Reserved	Reserved for future use
0x06-0x08	EEPROM	Factory EEPROM Control Registers
0x09-0x0A	Reserved	Reserved for future use
0x0B (Wr)	Dimmer	Display duty cycle from 0 to 100%: On time is (n x 100uS) + 100uS for a minimum illumination of 1% and a PWM frequency of 10Khz. 50% will be equal to a 10.1mS period of 50% duty cycle (~100Hz).
0x0C (Wr)	Delay	Delay in 10mS units from 10mS to 2.55S used for the free running burn-in counter mode (Count increment timer) as well as the character flash mode (On/Off timer).
0x0D (Wr)	Command	Command 0x01 Start burn-in counter 0x02 Stop burn-in counter 0x03 Start character flashing 0x04 Stop character flashing 0xF0 Querry state of address pins[1] 0xF1 Reset slave CPU
0x0E	FirmwareCore	Read Only: 0161
0x0F	FirmwareRevision	Read Only: VRR Variant (0/1/2) and Revision (00-99)

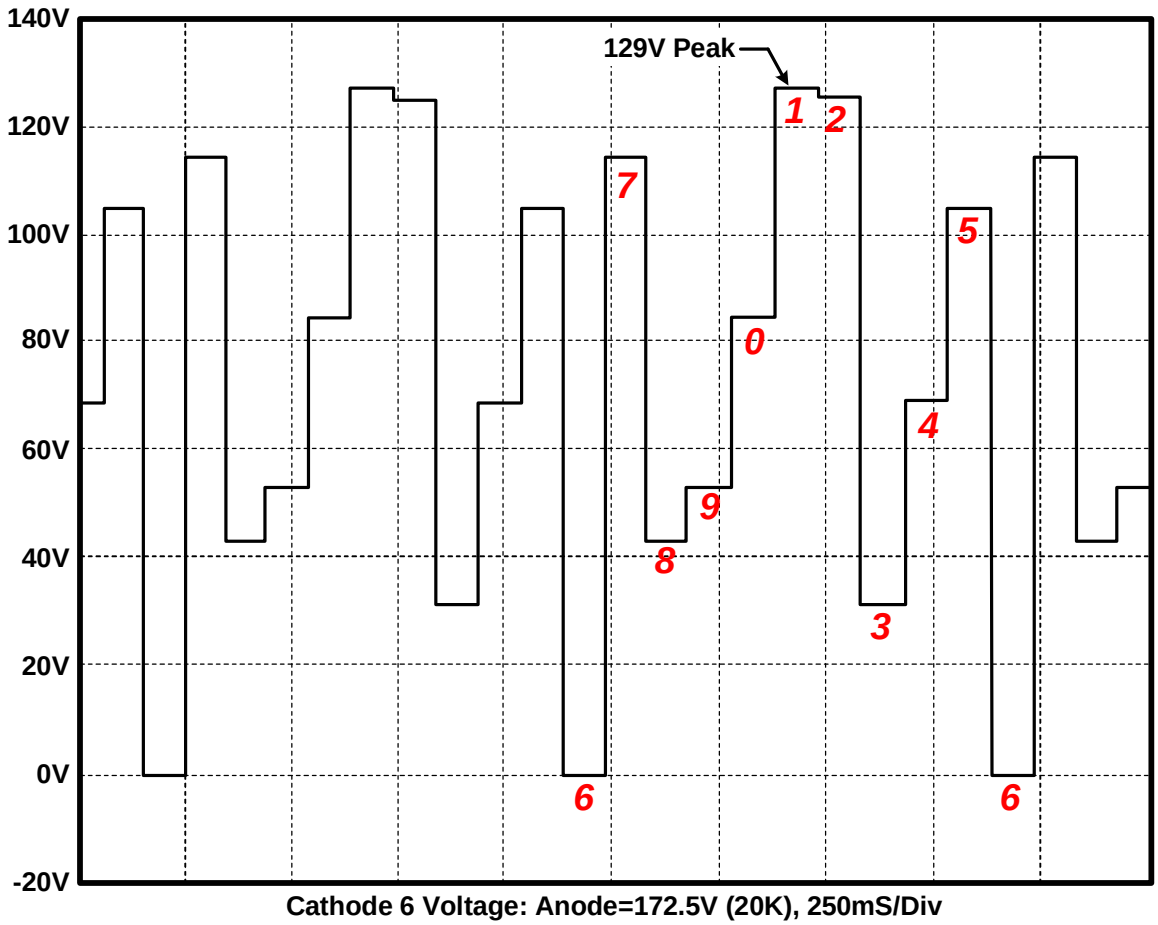
BitmapHigh / BitmapLow

BitmapHigh								BitmapLow									
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Nixie	Numitron
x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	1	"0"	Seg-A
x	x	x	x	0	0	0	0	0	0	0	0	0	0	1	0	"1"	Seg-B
x	x	x	x	0	0	0	0	0	0	0	0	0	1	0	0	"2"	Seg-C
x	x	x	x	0	0	0	0	0	0	0	0	1	0	0	0	"3"	Seg-D
x	x	x	x	0	0	0	0	0	0	0	1	0	0	0	0	"4"	Seg-E
x	x	x	x	0	0	0	0	0	0	1	0	0	0	0	0	"5"	Seg-F
x	x	x	x	0	0	0	0	0	1	0	0	0	0	0	0	"6"	Seg-G
x	x	x	x	0	0	0	0	1	0	0	0	0	0	0	0	"7"	Seg-DP
x	x	x	x	0	0	0	1	0	0	0	0	0	0	0	0	"8"	Spare-A
x	x	x	x	0	0	1	0	0	0	0	0	0	0	0	0	"9"	Spare-B
x	x	x	x	0	1	0	0	0	0	0	0	0	0	0	0	Spare 1	Spare 1
x	x	x	x	1	0	0	0	0	0	0	0	0	0	0	0	Spare 2	Spare 2

Notes:

1. The state of the A0-A3 pins are read and then put into register 0 for the next read transaction on register 0x00.

Section 5: SmartNixie Electrical



Cathode 6 Voltage: Anode=172.5V (20K), 250mS/Div

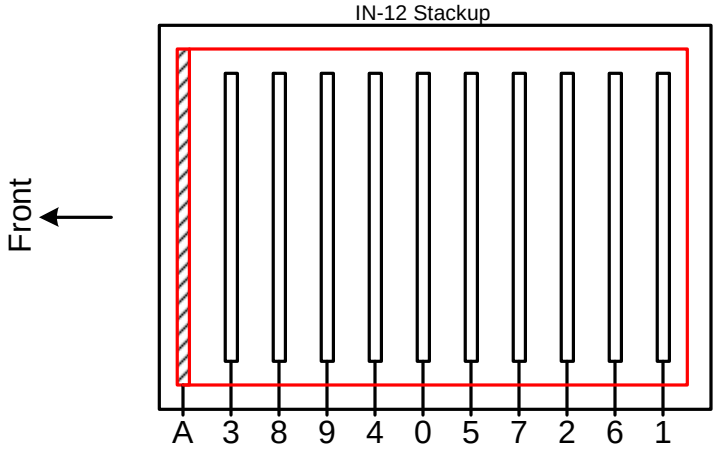


Figure 20: Burn-in Counting Mode Inter-Digit Coupling (-IN12 module signals shown)

Section 6: SmartNixie Mechanical

Figure 21: Package Outline, SmartNixie-IN4

Section 6: SmartNixie Mechanical

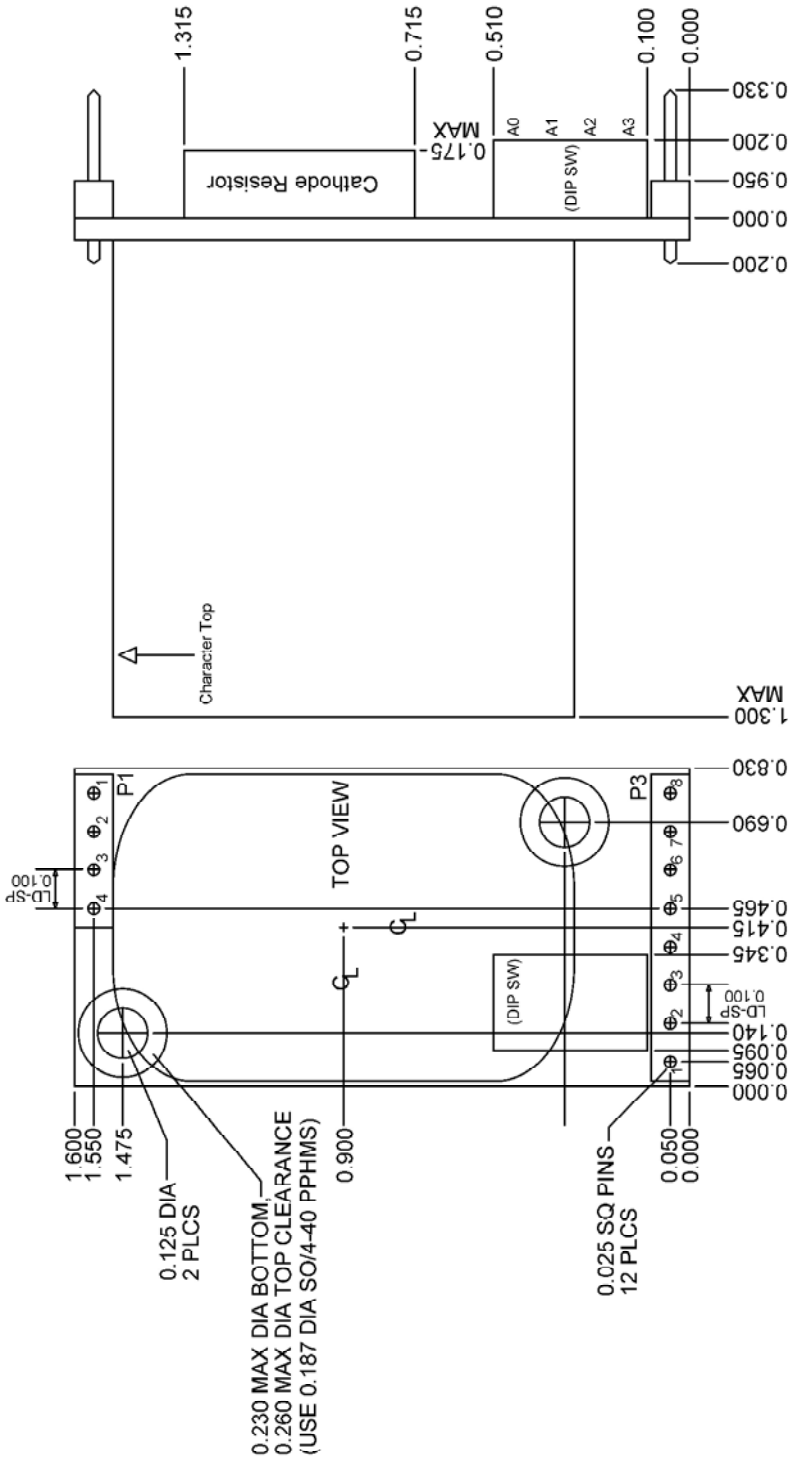


Figure 22: Package Outline, SmartNixie-IN12

Section 6: SmartNixie Mechanical

Figure 23: Package Outline, SmartNixie-IN17a

Section 6: SmartNixie Mechanical

Figure 24: Package Outline, SmartNixie-IN17b

Section 6: SmartNixie Mechanical

Figure 25: Package Outline, SmartNixie-IN18